

128M X 72 Bit (1GB) SDRAM Registered 168-Pin DIMM ECC (PC133); RoHS Compliant

FEATURES

- PC133 Compliant
(Option A: $t_{CYC} = 7.5ns@CL = 3$)
(Option D: $t_{CYC} = 7.5ns@CL = 2, 3$)
- Burst Mode Operation
- Auto and self refresh capability
(8192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V \pm 0.3V power supply
- MRS cycle with address key programs
 - Latency (access from column address)
 - Burst Length (1, 2, 4, 8, and Full Page)
 - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with 256 Byte EEPROM
- Optimized for ECC
- RoHS Compliant, lead free

GENERAL DESCRIPTION

The SL72R8P128M8H-A75xVU is a 128M x 72 bit Synchronous Dynamic RAM (SDRAM) Dual In-line Memory Module (DIMM).

The module consists of thirty-six CMOS 16M x 4 bit x 4 banks SDRAMs in 54-pin 400-mil TSOP-II packages. The SDRAMs are mounted in stacks of two on a 168-pin glass epoxy substrate using the patented IC Tower stacking technology.

A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). PLL circuits supply clocks to the SDRAMs. Decoupling capacitors are mounted. Control and address signals are registered.

The module has edge connections and is intended for mounting into 168-pin DIMM edge connector sockets keyed for 3.3V power supply. The module is PC133 compliant (see *Ordering Information* for options).

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	25	NC	49	VDD	73	VDD	97	DQ41	121	A9	145	NC
2	DQ0	26	VDD	50	NC	74	DQ28	98	DQ42	122	BA0	146	VREF*
3	DQ1	27	\overline{WE}	51	NC	75	DQ29	99	DQ43	123	A11	147	REGE
4	DQ2	28	DQM0	52	CB2	76	DQ30	100	DQ44	124	VDD	148	VSS
5	DQ3	29	DQM1	53	CB3	77	DQ31	101	DQ45	125	CLK1**	149	DQ53
6	VDD	30	\overline{CS}_0	54	VSS	78	VSS	102	VDD	126	A12	150	DQ54
7	DQ4	31	DU	55	DQ16	79	CLK2**	103	DQ46	127	VSS	151	DQ55
8	DQ5	32	VSS	56	DQ17	80	NC	104	DQ47	128	CKE0	152	VSS
9	DQ6	33	A0	57	DQ18	81	NC	105	CB4	129	\overline{CS}_3	153	DQ56
10	DQ7	34	A2	58	DQ19	82	SDA	106	CB5	130	DQM6	154	DQ57
11	DQ8	35	A4	59	VDD	83	SCL	107	VSS	131	DQM7	155	DQ58
12	VSS	36	A6	60	DQ20	84	VDD	108	NC	132	A13*	156	DQ59
13	DQ9	37	A8	61	NC	85	VSS	109	NC	133	VDD	157	VDD
14	DQ10	38	A10/AP	62	VREF*	86	DQ32	110	VDD	134	NC	158	DQ60
15	DQ11	39	BA1	63	CKE1	87	DQ33	111	\overline{CAS}	135	NC	159	DQ61
16	DQ12	40	VDD	64	VSS	88	DQ34	112	DQM4	136	CB6	160	DQ62
17	DQ13	41	VDD	65	DQ21	89	DQ35	113	DQM5	137	CB7	161	DQ63
18	VDD	42	CLK0	66	DQ22	90	VDD	114	\overline{CS}_1	138	VSS	162	VSS
19	DQ14	43	VSS	67	DQ23	91	DQ36	115	\overline{RAS}	139	DQ48	163	CLK3**
20	DQ15	44	DU	68	VSS	92	DQ37	116	VSS	140	DQ49	164	NC
21	CB0	45	\overline{CS}_2	69	DQ24	93	DQ38	117	A1	141	DQ50	165	SA0
22	CB1	46	DQM2	70	DQ25	94	DQ39	118	A3	142	DQ51	166	SA1
23	VSS	47	DQM3	71	DQ26	95	DQ40	119	A5	143	VDD	167	SA2
24	NC	48	DU	72	DQ27	96	VSS	120	A7	144	DQ52	168	VDD

* = Not Used. ** = CLK1-CLK3 are terminated.

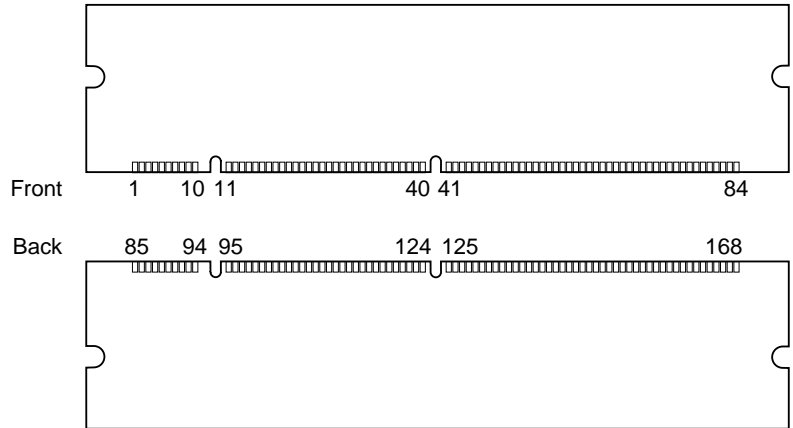
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PIN CONFIGURATION *(continued)*

Pin Functions

Pin Symbol	Pin Function
A0-A9, A11, A12	Address Inputs
A10/AP	Address Input/Autoprecharge
BA0, BA1	Bank Select Address Inputs
DQ0-DQ63	Data Inputs/Outputs
CB0-CB7	Check Bit Data Inputs/Outputs
\overline{WE}	Write Enable
CLK0-CLK3	Clock Inputs
CKE0, CKE1	Clock Enable Input
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
DQM0-DQM7	Data Input/Output Mask
$\overline{CS}0-\overline{CS}3$	Chip Select Inputs
REGE	Register Enable
SDA	Serial Data Input/Output
SCL	Serial Clock
SA0-SA2	Serial Address Inputs
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection
DU	Don't Use

Pin Arrangement

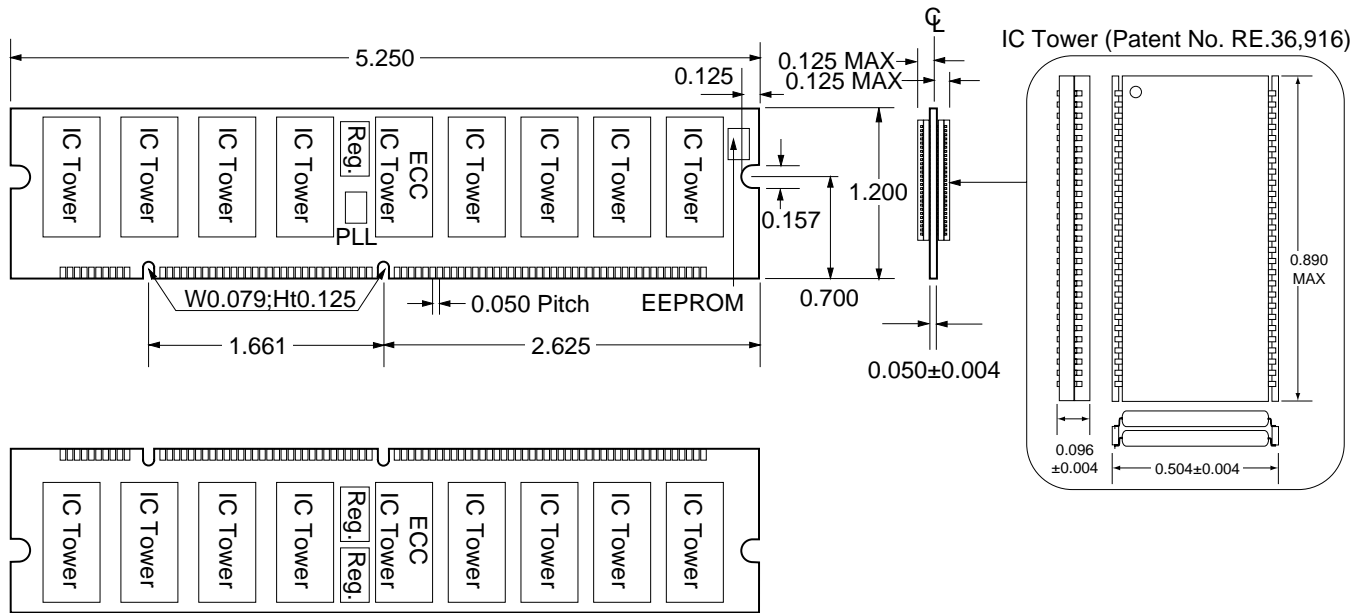


ORDERING INFORMATION

Part Number	PC133 133MHz Parameters				
	CL	tRCD	tRP	tRC	Comment
SL72R8P128M8H-A75AVU	3clks	20ns	20ns	67.5ns	Refer to option A in this specification.
SL72R8P128M8H-A75DVU	2clks	15ns	15ns	67.5ns	Refer to option D in this specification.

PACKAGE DIMENSIONS

Units: Inches



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

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SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I²C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

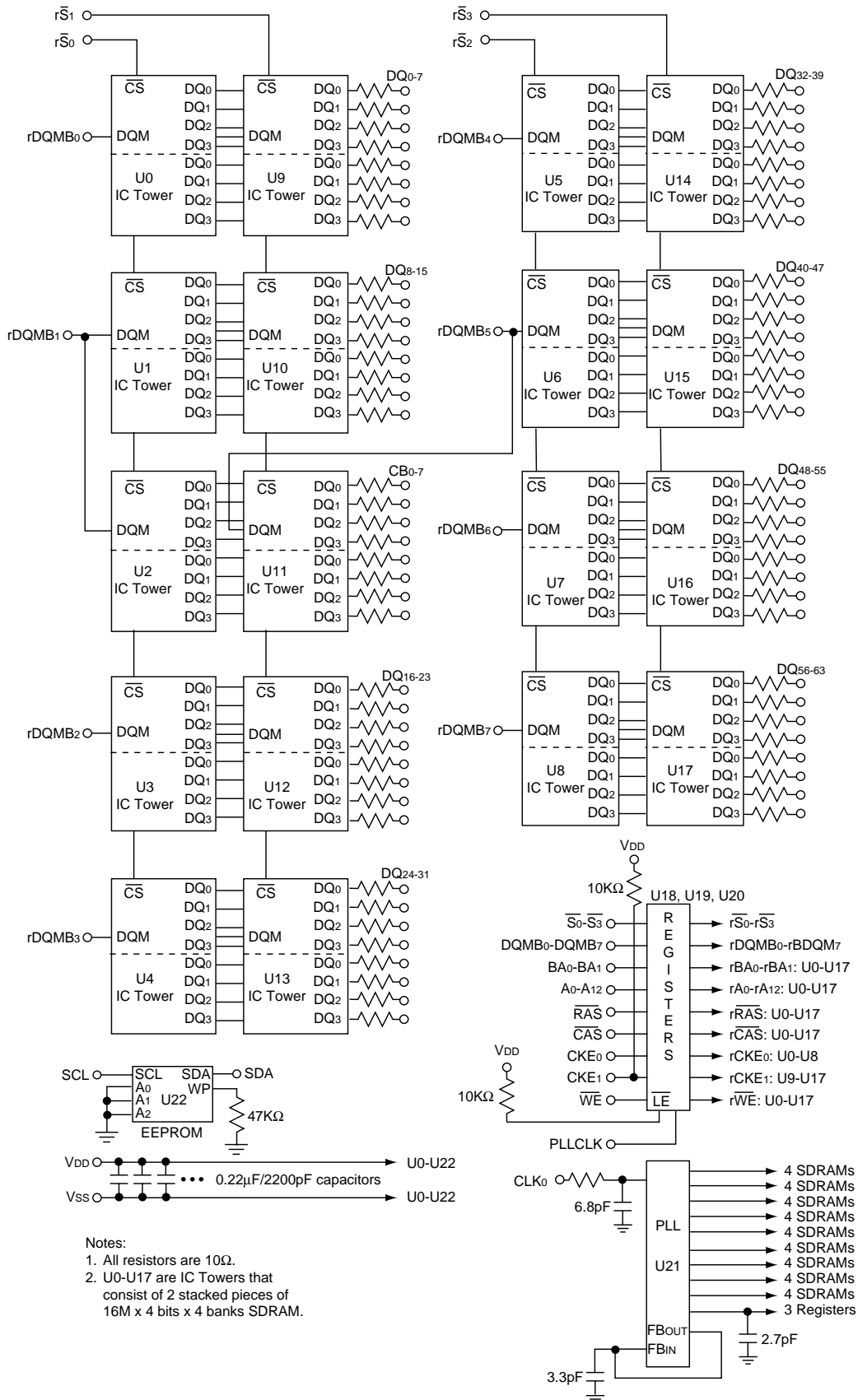
Byte #	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
0	# of bytes written into serial memory at module manufacturer	128 bytes		80h	
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)		08h	
2	Fundamental memory type	SDRAM		04h	
3	# of row addresses on this assembly	13		0Dh	
4	# of column addresses on this assembly	11		0Bh	
5	# of module banks on this assembly	2 banks		02h	
6	Data width of this assembly	72 bits		48h	
7	...Data width of this assembly (continued)	—		00h	
8	Voltage interface standard of this assembly	LVTTL		01h	
9	SDRAM cycle time at CL=3 (tCYC)	7.5ns	7.5ns	75h	75h
10	SDRAM access time from clock at CL=3 (tAC)	5.4ns	5.4ns	54h	54h
11	DIMM configuration type	ECC		02h	
12	Refresh rate/type	7.8µs, Self-refresh		82h	
13	SDRAM width	4 bits		04h	
14	Error Checking DRAM data width	4 bits		04h	
15	Min. CLK delay for back-to-back rand. col. addr.	tCCD=1 CLK		01h	
16	SDRAM device attributes: burst lengths supported	1,2,4,8, and Full Page		8Fh	
17	SDRAM device attributes: # of banks on SDRAM device	4 banks		04h	
18	SDRAM device attributes: CAS latency	CAS latency = 2,3		06h	
19	SDRAM device attributes: CS latency	CS latency = 0		01h	
20	SDRAM device attributes: Write latency	Write Latency = 0		01h	
21	SDRAM module attributes	Registered/Buffered/PLL		1Fh	
22	SDRAM device attributes: general	VCC10%, B/R, S/W, P/A, A/P		0Eh	
23	Minimum clock cycle time at CL=2 (tCYC)	10ns	75ns	A0h	75h
24	Max. data access time form clock at CL=2 (tAC)	6ns	5.4ns	60h	54h
25	Minimum clock cycle time at CL=1 (tCYC)	—	—	00h	00h
26	Max. data access time from clock at CL=1 (tAC)	—	—	00h	00h
27	Minimum row precharge time (tRP)	20ns	15ns	14h	0Fh
28	Minimum row active to row active delay (tRRD)	15ns	15ns	0Fh	0Fh
29	Minumum RAS to CAS (tRCD)	20ns	15ns	14h	0Fh
30	Minumum RAS pulse width (tRAS)	45ns	45ns	2Dh	2Dh
31	Module bank density	512MB		80h	
32	Min. command and address signal setup time (tAS)	1.5ns		15h	
33	Min. command and address signal hold time (tAH)	0.8ns		08h	
34	Min. data signal input setup time (tDS)	1.5ns		15h	
35	Min. data signal input hold time (tDH)	0.8ns		08h	

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SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte #	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
36-61	Superset information (may be used in future)	—		00h	
62	SPD revision	1.2		12h	
63	Checksum for bytes 0-62	JEDEC Calculation		xxh	
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code		7Fh	
65	Man. JEDEC ID code (continued)	STEC's ID		A8h	
66-71	—	—		00h	
72	Manufacturing location	STEC USA/Malaysia		01h/02h	
73-90	Manufacturer's part number			xxh	
91	Revision code of PCB	Rev A		01h	
92	—			00h	
93	Manufacturing date	Year (BCD)		yy	
94		Calender Week (BCD)		w w	
95	Assembly serial number	Tester number		ss	
96		Serial number (bits 7-0)		ss	
97		Serial number (bits 15-8)		ss	
98		Serial number (bits 23-16)		ss	
99-125	Manufacturer's specific data			xxh	
126	Intel specification frequency	100MHz		64h	
127	Intel specification details	1000-1111		8Fh	
128-255	Unused storage locations	—		FFh	

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to VSS	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on VCC Supply Relative to VSS	V _{DD}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +125	°C
Operating Temperature (ambient)	T _{opr}	0 to +70	°C
Power Dissipation	P _D	36	W
Short Circuit Output Current	I _{OS}	±50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to VSS, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V _{DD}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	0	0.8	V	2
Output High Voltage Level	V _{OH}	2.4	—	—	V	I _{OH} =-2mA
Output Low Voltage Level	V _{OL}	—	—	0.4	V	I _{OL} =2mA
Input Leakage Current (Inputs)	I _{IL}	-5	—	5	μA	3
Input Leakage Current (I/O)	I _{IL}	-10	—	10	μA	3,4

1. V_{IH}(max)=5.6V AC. The overshoot voltage duration is ≤3ns.
2. V_{IL}(min)=-2.0V AC. The undershoot voltage duration is ≤3ns.
3. Any input 0≤V_{IN}≤V_{DD}.
4. Data out is disabled, 0≤V_{OUT}≤V_{DD}).

CAPACITANCE (V_{DD}=3.3V, T_A=25 °C, f=1MHz)

Item	Symbol	Max	Units
Input Capacitance (address, \overline{WE} , \overline{RAS} , \overline{CAS})	C11	16	pF
Input Capacitance (DQM0-DQM7)	C12	16	pF
Input Capacitance ($\overline{CS}0$ - $\overline{CS}3$)	C13	16	pF
Input Capacitance (CLK ₀)	C14	16	pF
Input Capacitance (CKE ₀ , CKE ₁)	C15	16	pF
Input Capacitance (REGE)	C16	16	pF
Input/Output Capacitance (DQ ₀ -DQ ₆₃ , CB ₀ -CB ₇)	C _{I/O1}	22	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted. TA=0 to 70°C)

Parameter	Symbol	Test Condition	Max	Units	
Operating Current (One Bank Active)	ICC1S	Burst length=1, t _{RC} >=t _{RC} (min), I _{OL} =0mA, Outputs open	Option A Option D 2200 2380	mA	
Precharge Standby Current in Power-Down Mode	ICC2P	CKE<=V _{IL} (max), t _{CLK} =10ns,	112	mA	
	ICC2PS	CKE and CLK<=V _{IL} (max), t _{CLK} =infinity	72	mA	
Precharge Standby Current in Non Power-Down Mode	ICC2N	CKE and S>=V _{IH} (min), t _{CLK} =10ns Input signals are changed one time during two clocks	760	mA	
	ICC2NS	CKE>=V _{IH} (min), CLK<=V _{IL} (max), t _{CLK} =infinity Input signals are stable	360	mA	
Active Standby Current in Power-Down Mode	ICC3P	CKE<=V _{IL} (max), t _{CLK} =10ns	256	mA	
	ICC3PS	CKE and CLK<=V _{IL} (max), t _{CLK} =infinity	216	mA	
Active Standby Current in Non Power-Down Mode (One Bank Active)	ICC3N	CKE and S>=V _{IH} (min), t _{CLK} =10ns, Input signals are changed one time during two clocks	1120	mA	
	ICC3NS	CKE>=V _{IH} (min), CLK<=V _{IL} (max), t _{CLK} =infinity Inputs are stable	900	mA	
Operating Current (Burst Mode)	ICC4	I _{OL} =0mA, Full Page I _{CCD} =2 CLKs, Outputs open, 4 banks activated	2560	mA	
Refresh Current (Refresh Period is 64ms)	ICC5	t _{RC} >=t _{RC} (min)	Option A	3640	mA
			Option D	4540	mA
Self Refresh Current	ICC6	CKE<=0.2V	148	mA	

AC TIMING PARAMETERS (TA=0-65°C; VCC=3.0V-3.6V; CL=2, 3)

Parameter	Symbol	Speed Grade 100MHz		Speed Grade 133MHz/100MHz		Unit	Notes
		Min	Max	Min	Max		
Clock Period	tCLK	10		7.5		ns	
Clock High Time (Rated @1.5V)	tCH	3		2.5		ns	
Clock Low Time	tCL	3		2.5		ns	
Input Setup Times (Data) (Address/Command & CKE)	tSI	2		1.5		ns	
Input Hold Times (Data) (Address/Command & CKE)	tHI	1		0.8		ns	
Output Valid From Clock (CL=2; limited application; 2 banks; all outputs switching)	tAC		7.0		N/A	ns	1
Output Valid From Clock (CL=2; LVTTTL levels; Rated@50pF; all outputs switching)	tAC		6.0 (tCO=5.2)		5.4 (tCO=4.6)	ns	1
Output Valid From Clock (CL=3; LVTTTL levels; Rated@50pF; all outputs switching)	tAC		6.0 (tCO=5.2)		5.4 (tCO=4.6)	ns	1
Output Hold From Clock (Rated@50pF; 1.8ns@0pF)	tOH	3		2.7		ns	
Output Valid to Z	tOHZ	3	9	2.7	7	ns	
CAS to CAS Delay	tCCD	1		1		tCLK	
CAS Bank Delay	tCBD	1		1		tCLK	
CKE to Clock Disable	tCKE	1		1		tCLK	
RAS Precharge Time Option D/A	tRP	15.0/20.0		15.0/20.0		ns	
RAS Active Time	tRAS	50		45		ns	
Active to Command Delay (RAS to CAS Delay) Option D/A	tRCD	15.0/20.0		15.0/20.0		ns	
RAS to RAS Bank Activate Delay	tRRD	20		15		ns	
RAS Cycle Time	tRC	70		67.5		ns	
DQM to Input Data Delay	tDQD	0		0		tCLK	
Write Cmd. to Input Data Delay	tDWD	0		0		tCLK	
Mode Register Set to Active Delay	tMRD	3		3		tCLK	
Precharge to O/P in High-Z	tROH		CL		CL	tCLK	2
DQM to Data in Hi-Z for Read	tDQZ	2		2		tCLK	
DQM to Data Mask for Write	tDQM	0		0		tCLK	3
Data-In to PRE Command Period	tDPL	20		15		ns	
Data-In to ACT (PRE) Cmd Period (Auto Precharge)	tDAL	5		5		tCLK	
Power Down Mode Entry	tSB		1		1	tCLK	
Self Refresh Exit Time	tSRX	10		10		ns	4
Power Down Exit Set Up Time	tPDE	1		1		tCLK	5
Clock Stop During Self Refresh or Power Down	tCLKSTP	200		200		tCLK	6
Refresh Period	tREF		64		64	ms	7
Row Refresh Cycle Time	tRFC	80.0		75.0		ns	

- Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V. tACN=access time with 0pF load.
- CL=CAS Latency.
- Data Masked on the same clock.
- Self refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + tRC.
- Timing is asynchronous. If tset is not met by rising edge of CLK then CKE is assumed latched on next cycle.
- If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
- For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit technology, 8192 refresh cycles.

REVISION HISTORY

Rev. Change Description from Previous Revision

- 104 08/24/2007. U added to part number.
- 105 12/10/2007. Updated to latest format.

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