

32M X 72 Bits (256MB) 144-Pin SDRAM SO-DIMM with ECC (PC133)

FEATURES

- PC133 Compliant
(Option A: $t_{CYC}=7.5ns@CL=3$)
(Option D: $t_{CYC}=7.5ns@CL=2,3$)
- Burst Mode Operation
- Auto and self refresh capability
(8192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V \pm 0.3V power supply
- MRS cycle with address key programs
 - Latency (access from column address)
 - Burst Length (1, 2, 4, 8)
 - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with 256 Byte EEPROM
- ECC
- RoHS Compliant, lead-free version available

GENERAL DESCRIPTION

The SL72G8F32M8H-A75xV(U) is a 32M x 72 bits Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of nine 8M x 8 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP II packages mounted on a 144-pin glass epoxy substrate.

A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1 μ F are mounted. Damping resistors are mounted for the data lines. A PLL supplies clocks to the SDRAMs from one clock input.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

See *Ordering Information* for PC133 performance options.

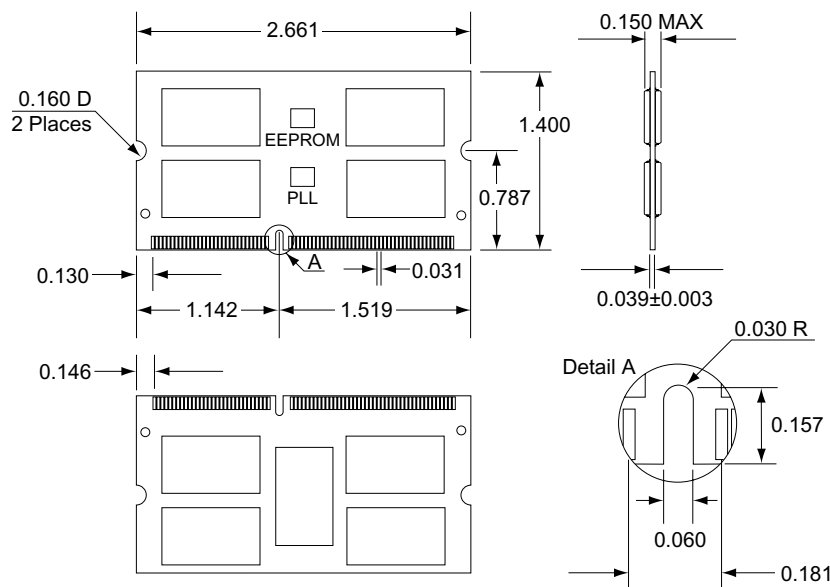
ORDERING INFORMATION

Part Number	PC133 133MHz Parameters				Comment
	CL	t _{RCD}	t _{RP}	t _{RC}	
SL72G8F32M8H-A75AV(U)	3clks	20ns	20ns	67.5ns	Refer to option A in this specification
SL72G8F32M8H-A75DV(U)	2clks	15ns	15ns	67.5ns	Refer to option D in this specification

Note:The "U" in the part number selects the RoHS Compliant, lead-free version of the module.

PACKAGE DIMENSIONS

Units are in inches. Tolerances are ± 0.005 unless otherwise specified.



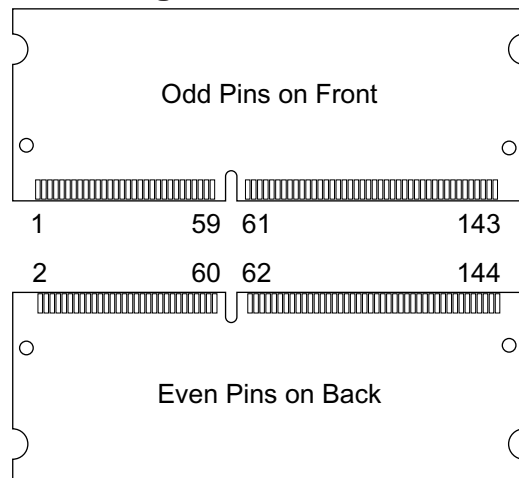
PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	21	VSS	41	DQ10	61	CLK0	81	VDD	101	VDD	121	DQ24	141	SDA
2	VSS	22	VSS	42	DQ42	62	CKE0	82	VDD	102	VDD	122	DQ56	142	SCL
3	DQ0	23	DQMB0	43	DQ11	63	VDD	83	DQ16	103	A6	123	DQ25	143	VDD
4	DQ32	24	DQMB4	44	DQ43	64	VDD	84	DQ48	104	A7	124	DQ57	144	VDD
5	DQ1	25	DQMB1	45	VDD	65	$\overline{\text{RAS}}$	85	DQ17	105	A8	125	DQ26		
6	DQ33	26	DQMB5	46	VDD	66	$\overline{\text{CAS}}$	86	DQ49	106	BA0	126	DQ58		
7	DQ2	27	VDD	47	DQ12	67	$\overline{\text{WE}}$	87	DQ18	107	VSS	127	DQ27		
8	DQ34	28	VDD	48	DQ44	68	CKE1*	88	DQ50	108	VSS	128	DQ59		
9	DQ3	29	A0	49	DQ13	69	$\overline{\text{S}}_0$	89	DQ19	109	A9	129	VDD		
10	DQ35	30	A3	50	DQ45	70	A12	90	DQ51	110	BA1	130	VDD		
11	VDD	31	A1	51	DQ14	71	$\overline{\text{S}}_1^*$	91	VSS	111	A10/AP	131	DQ28		
12	VDD	32	A4	52	DQ46	72	A13*	92	VSS	112	A11	132	DQ60		
13	DQ4	33	A2	53	DQ15	73	NC	93	DQ20	113	VDD	133	DQ29		
14	DQ36	34	A5	54	DQ47	74	CLK1*	94	DQ52	114	VDD	134	DQ61		
15	DQ5	35	VSS	55	VSS	75	VSS	95	DQ21	115	DQMB2	135	DQ30		
16	DQ37	36	VSS	56	VSS	76	VSS	96	DQ53	116	DQMB6	136	DQ62		
17	DQ6	37	DQ8	57	CB0	77	CB2	97	DQ22	117	DQMB3	137	DQ31		
18	DQ38	38	DQ40	58	CB4	78	CB6	98	DQ54	118	DQMB7	138	DQ63		
19	DQ7	39	DQ9	59	CB1	79	CB3	99	DQ23	119	VSS	139	VSS		
20	DQ39	40	DQ41	60	CB5	80	CB7	100	DQ55	120	VSS	140	VSS		

* Not used

Pin Arrangement

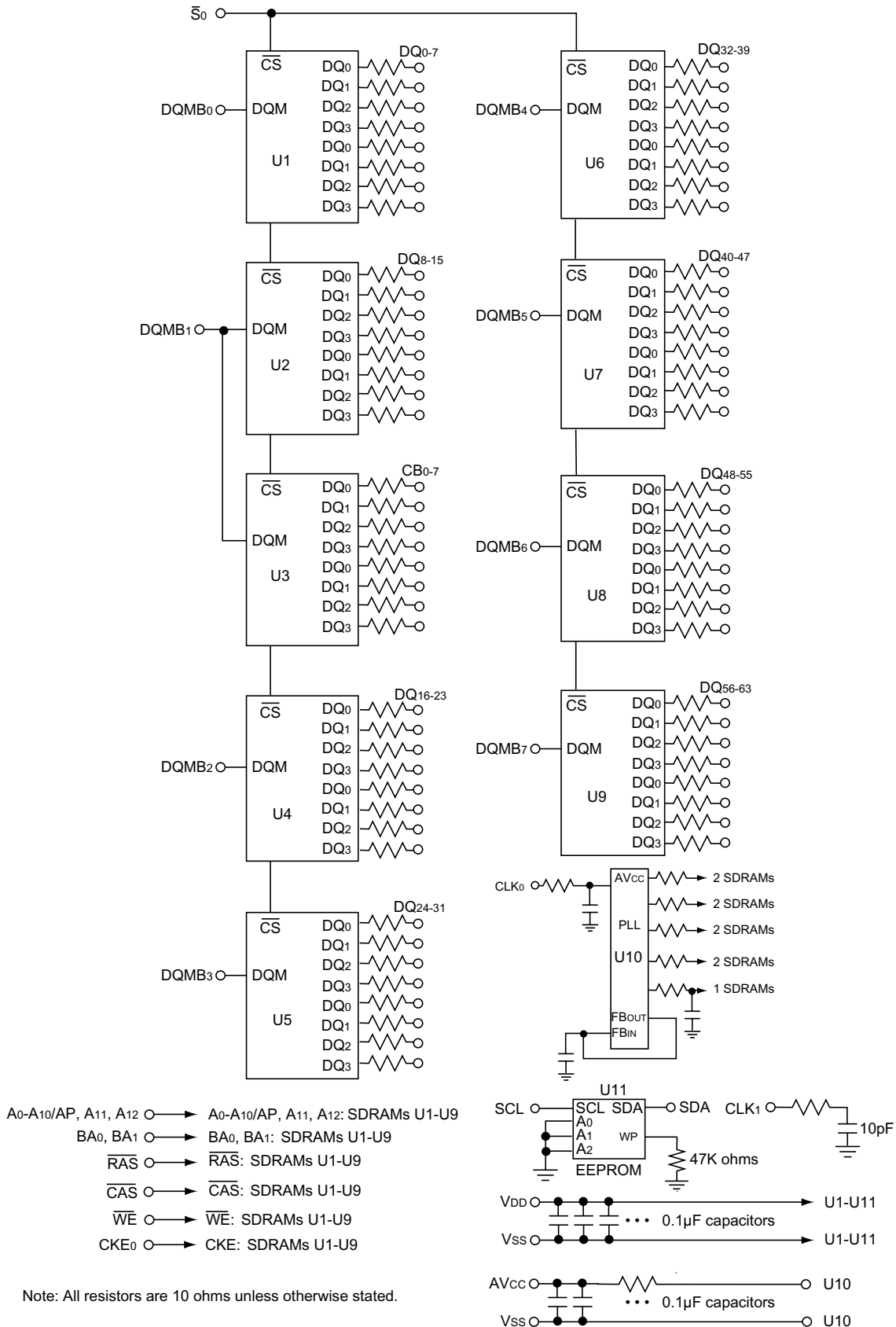


Pin Functions

Pin Name	Pin Function
A0-A10/AP, A11, A12	Address Inputs (multiplexed)
BA0, BA1	Select Bank
DQ0-DQ63	Data In/Out
CB0-CB7	Check Bits
$\overline{\text{WE}}$	Read/Write Enable
CLK0	Clock Input
CKE0	Clock Enable Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQMB0-DQMB7	Data Input/Output Mask
$\overline{\text{S}}_0$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

(Where x selects PC133 CAS Latency; U = RoHS Compliant, lead free version.)

FUNCTIONAL BLOCK DIAGRAM



SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I²C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
0	# of bytes written into serial memory at module manufacturer	128 bytes		80h	
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)		08h	
2	Fundamental memory type	SDRAM		04h	
3	# of row addresses on this assembly	13		0Dh	
4	# of column addresses on this assembly	10		0Ah	
5	# of module banks on this assembly	1 bank		01h	
6	Data width of this assembly	72 bits		48h	
7	...Data width of this assembly (continued)	—		00h	
8	Voltage interface standard of this assembly	LVTTL		01h	
9	SDRAM cycle time at CL=3 (tCYC)	7.5ns	7.5ns	75h	75h
10	SDRAM access time from clock at CL=3 (tAC)	5.4ns	5.4ns	54h	54h
11	DIMM configuration type	ECC		02h	
12	Refresh rate/type	7.8µs, Self-refresh		82h	
13	SDRAM width	8 bits		08h	
14	Error Checking DRAM data width	8 bits		08h	
15	Min. CLK delay for back-to-back rand. col. addr.	tCCD=1 CLK		01h	
16	SDRAM device attributes: burst lengths supported	1,2,4,8		0Fh	
17	SDRAM device attributes: # of banks on SDRAM device	4 banks		04h	
18	SDRAM device attributes: CAS latency	CAS latency = 2,3		06h	
19	SDRAM device attributes: CS latency	CS latency = 0		01h	
20	SDRAM device attributes: Write latency	Write Latency = 0		01h	
21	SDRAM module attributes	on-card PLL, non-buff., non-reg.		04h	
22	SDRAM device attributes: general	VCC10%, B/R, S/W, P/A, A/P		0Eh	
23	Minimum clock cycle time at CL=2 (tCYC)	10ns	75ns	A0h	75h
24	Max. data access time form clock at CL=2 (tAC)	6ns	5.4ns	60h	54h
25	Minimum clock cycle time at CL=1 (tCYC)	—	—	00h	00h
26	Max. data access time from clock at CL=1 (tAC)	—	—	00h	00h
27	Minimum row precharge time (tRP)	20ns	15ns	14h	0Fh
28	Minimum row active to row active delay (tRRD)	15ns	15ns	0Fh	0Fh
29	Minumum RAS to CAS (tRCD)	20ns	15ns	14h	0Fh
30	Minumum RAS pulse width (tRAS)	45ns	45ns	2Dh	2Dh
31	Module bank density	256MB		40h	
32	Min. command and address signal setup time (tAS)	1.5ns		15h	
33	Min. command and address signal hold time (tAH)	0.8ns		08h	
34	Min. data signal input setup time (tDS)	1.5ns		15h	

(Serial Presence Detect Information continued on the next page)

SERIAL PRESENCE DETECT INFORMATION (continued)

Byte #	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
35	Min. data signal input hold time (TDH)	0.8ns		08h	
36-61	Superset information (may be used in future)	—		00h	
62	SPD revision	1.2		12h	
63	Checksum for bytes 0-62	JEDEC calculation		xxh	
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code		7Fh	
65	Man. JEDEC ID code (continued)	STEC's ID		A8h	
66-71				00h	
72	Manufacturing location	STEC USA		01h	
73-90	Manufacturer's part number			xxh	
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)		01h	
92				00h	
93	Manufacturing date	Year (BCD)		yy	
94		Calender Week (BCD)		w w	
95	Assembly serial number	Tester number		ss	
96		Serial number (bits 7-0)		ss	
97		Serial number (bits 15-8)		ss	
98		Serial number (bits 23-16)		ss	
99-125	Manufacturer's specific data			xxh	
126	Intel specification frequency	100MHz		64h	
127	Intel specification details	Detailed 100MHz Info		8Fh	

ABSOLUTE MAXIMUM RATINGS¹

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to VSS	V _{IN} , V _{OUT}	-1.0 to +4.6	V
Voltage on VCC Supply Relative to VSS	V _{DD}	-1.0 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	9	W
Short Circuit Output Current	I _{OS}	50	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to VSS=0, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V _{DD}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	0	0.8	V	2
Output High Voltage Level	V _{OH}	2.4	—	—	V	I _{OH} =-2mA
Output Low Voltage Level	V _{OL}	—	—	0.4	V	I _{OL} =2mA
Input Leakage Current	I _{IL}	-90	—	90	µA	3

1. V_{IH}(max)=5.6 V AC (pulse width <=3 ns acceptable)
2. V_{IL}(min) = -2.0 V AC (pulse width <=3 ns acceptable)
3. Any input 0<=V_{IN}<=V_{DD}.

CAPACITANCE (T_A=23 °C, V_{DD}=3.3V, f=1MHz, V_{REF}=1.4±200mA)

Item	Symbol	Max	Units
Input Capacitance (A ₀ -A ₁₀ /AP, A ₁₁ , A ₁₂ , BA ₀ , BA ₁)	C _{IN1}	45	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{WE})	C _{IN2}	45	pF
Input Capacitance (CLK ₀)	C _{IN3}	12	pF
Input Capacitance (CKE ₀)	C _{IN4}	45	pF
Input Capacitance ($\overline{S_0}$)	C _{IN5}	45	pF
Input Capacitance (DQMB ₀ , DQMB ₂ -DQMB ₇)	C _{IN6}	14	pF
Input Capacitance (DQMB ₁)	C _{IN7}	18	pF
Input/Output Capacitance (DQ ₀ -DQ ₆₃)	C _{IO1}	16.5	pF

(Where x selects PC133 CAS Latency; U = RoHS Compliant, lead free version.)

DC CHARACTERISTICS

Recommended operating conditions unless otherwise noted. TA=0 to 70°C.

Parameter	Symbol	Test Condition	Max	Units
Operating Current (One Bank Active)	ICC1S	Burst length=1, t _{RC} >=t _{RC} (min), I _{OL} =0mA, Outputs open	Option A Option D 990 1080	mA
Precharge Standby Current in Power-Down Mode	ICC2P	CKE<=V _{IL} (max), t _{CLK} =10ns,	18	mA
	ICC2PS	CKE and CLK<=V _{IL} (max), t _{CLK} =infinity	18	mA
Precharge Standby Current in Non Power-Down Mode	ICC2N	CKE and S>=V _{IH} (min), t _{CLK} =10ns Input signals are changed one time during 20ns	180	mA
	ICC2NS	CKE>=V _{IH} (min), CLK<=V _{IL} (max), t _{CLK} =infinity Input signals are stable	90	mA
Active Standby Current in Power-Down Mode	ICC3P	CKE<=V _{IL} (max), t _{CLK} =10ns	54	mA
	ICC3PS	CKE and CLK<=V _{IL} (max), t _{CLK} =infinity	54	mA
Active Standby Current in Non Power-Down Mode (One Bank Active)	ICC3N	CKE and S>=V _{IH} (min), t _{CLK} =10ns, Input signals are changed one time during 20ns	270	mA
	ICC3NS	CKE>=V _{IH} (min), CLK<=V _{IL} (max), t _{CLK} =infinity Inputs are stable	225	mA
Operating Current (Burst Mode)	ICC4	I _{OL} =0mA, BL=8, 4 banks activated ICCD=2 CLKs, Outputs open	1170	mA
Refresh Current (Refresh Period is 64ms)	ICC5	t _{RC} >=t _{RC} (min)	Option A Option D 1800 1980	mA
Self Refresh Current	ICC6	CKE<=0.2V	27	mA

AC TIMING PARAMETERS (T_A=0-65°C; V_{CC}=3.0V-3.6V; CL=2, 3)

Parameter	Symbol	Speed Grade 100MHz		Speed Grade 133MHz/100MHz		Unit	Notes
		Min	Max	Min	Max		
Clock Period	t _{CLK}	10		7.5		ns	
Clock High Time (Rated @1.5V)	t _{CH}	3		2.5		ns	
Clock Low Time	t _{CL}	3		2.5		ns	
Input Setup Times (Data) (Address/Command & CKE)	t _{SI}	2		1.5		ns	
Input Hold Times (Data) (Address/Command & CKE)	t _{HI}	1		0.8		ns	
Output Valid From Clock (CL=2; limited application; 2 banks; all outputs switching)	t _{AC}		7.0		N/A	ns	1
Output Valid From Clock (CL=2; LVTTTL levels; Rated@50pF; all outputs switching)	t _{AC}		6.0 (t _{CO} =5.2)		5.4 (t _{CO} =4.6)	ns	1
Output Valid From Clock (CL=3; LVTTTL levels; Rated@50pF; all outputs switching)	t _{AC}		6.0 (t _{CO} =5.2)		5.4 (t _{CO} =4.6)	ns	1
Output Hold From Clock (Rated@50pF; 1.8ns@0pF)	t _{OH}	3		2.7		ns	
Output Valid to Z	t _{OHZ}	3	9	2.7	7	ns	
CAS to CAS Delay	t _{CCD}	1		1		t _{CLK}	
CAS Bank Delay	t _{CBD}	1		1		t _{CLK}	
CKE to Clock Disable	t _{CKE}	1		1		t _{CLK}	
RAS Precharge Time	t _{RP}	15.0/20.0		15.0/20.0		ns	
RAS Active Time	t _{RAS}	50		45		ns	
Active to Command Delay (RAS to CAS Delay)	t _{RCD}	15.0/20.0		15.0/20.0		ns	
RAS to RAS Bank Activate Delay	t _{R RD}	20		15		ns	
RAS Cycle Time	t _{RC}	70		67.5		ns	
DQM to Input Data Delay	t _{DQD}	0		0		t _{CLK}	
Write Cmd. to Input Data Delay	t _{DWD}	0		0		t _{CLK}	
Mode Register Set to Active Delay	t _{M RD}	3		3		t _{CLK}	
Precharge to O/P in High-Z	t _{ROH}		CL		CL	t _{CLK}	2
DQM to Data in Hi-Z for Read	t _{DQZ}	2		2		t _{CLK}	
DQM to Data Mask for Write	t _{DQM}	0		0		t _{CLK}	3
Data-In to PRE Command Period	t _{DPL}	20		15		ns	
Data-In to ACT (PRE) Cmd Period (Auto Precharge)	t _{DAL}	5		5		t _{CLK}	
Power Down Mode Entry	t _{SB}		1		1	t _{CLK}	
Self Refresh Exit Time	t _{SRX}	10		10		ns	4
Power Down Exit Set Up Time	t _{PDE}	1		1		t _{CLK}	5
Clock Stop During Self Refresh or Power Down	t _{CLKSTP}	200		200		t _{CLK}	6
Refresh Period (4096 refresh cycles)	t _{REF}		64		64	ms	7
Row Refresh Cycle Time	t _{RFC}	80.0		75.0		ns	

1. Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V.
t_{ACN}=access time with 0pF load.

2. CL=CAS Latency.

3. Data Masked on the same clock.

4. Self refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + t_{RC}.

5. Timing is asynchronous. If t_{set} is not met by rising edge of CLK then CKE is assumed latched on next cycle.

6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.

7. For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit technology, 8192 refresh cycles.

REVISION HISTORY

Rev. **Change Description from Previous Revision**

- 105 10/13/2006. U option added.
- 106 08/13/2007. Updated logo, web address and SPD.