

64M X 32 Bits (256MB) 144-Pin SDRAM SO-DIMM (PC100)

FEATURES

- PC100 Compliant
(see *Ordering Information* for options)
- Burst Mode Operation
- Auto and self refresh capability
(8192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- MRS cycle with address key programs
 - Latency (access from column address)
 - Burst Length (1, 2, 4, and 8)
 - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- RoHS Compliant, lead-free

GENERAL DESCRIPTION

The SL32G8P64M8G-A10xVU is a 64M x 32 bits Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of eight CMOS 16M x 4 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP II packages mounted in stacks of two on a 144-pin glass epoxy substrate. The stacking technology is patented by STEC under patent number RE.36,916.

A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1µF are mounted for the SDRAMs and the EEPROM. Damping resistors are mounted for the data lines.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

See *Ordering Information* for PC100 performance options.

PIN CONFIGURATION

Pin Symbols

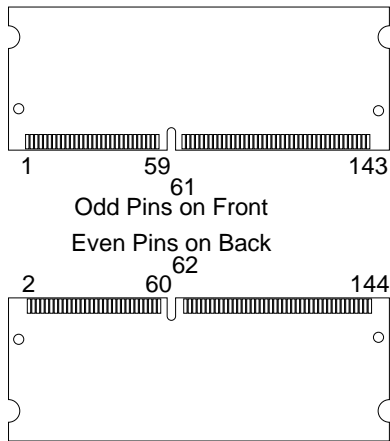
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	21	V _{SS}	41	DQ ₁₀	61	CLK ₀	81	V _{DD}	101	V _{DD}	121	DQ ₂₄	141	SDA
2	V _{SS}	22	V _{SS}	42	DQ ₄₂ *	62	CKE ₀	82	V _{DD}	102	V _{DD}	122	DQ ₅₆ *	142	SCL
3	DQ ₀	23	DQMB ₀	43	DQ ₁₁	63	V _{DD}	83	DQ ₁₆	103	A ₆	123	DQ ₂₅	143	V _{DD}
4	DQ ₃₂ *	24	DQMB ₄ *	44	DQ ₄₃ *	64	V _{DD}	84	DQ ₄₈ *	104	A ₇	124	DQ ₅₇ *	144	V _{DD}
5	DQ ₁	25	DQMB ₁	45	V _{DD}	65	\overline{RAS}	85	DQ ₁₇	105	A ₈	125	DQ ₂₆		
6	DQ ₃₃ *	26	DQMB ₅ *	46	V _{DD}	66	\overline{CAS}	86	DQ ₄₉ *	106	BA ₀	126	DQ ₅₈ *		
7	DQ ₂	27	V _{DD}	47	DQ ₁₂	67	\overline{WE}	87	DQ ₁₈	107	V _{SS}	127	DQ ₂₇		
8	DQ ₃₄ *	28	V _{DD}	48	DQ ₄₄ *	68	CKE ₁ *	88	DQ ₅₀ *	108	V _{SS}	128	DQ ₅₉ *		
9	DQ ₃	29	A ₀	49	DQ ₁₃	69	\overline{S}_0	89	DQ ₁₉	109	A ₉	129	V _{DD}		
10	DQ ₃₅ *	30	A ₃	50	DQ ₄₅ *	70	A ₁₂	90	DQ ₅₁ *	110	BA ₁	130	V _{DD}		
11	V _{DD}	31	A ₁	51	DQ ₁₄	71	\overline{S}_1 *	91	V _{SS}	111	A _{10/AP}	131	DQ ₂₈		
12	V _{DD}	32	A ₄	52	DQ ₄₆ *	72	A ₁₃ *	92	V _{SS}	112	A ₁₁	132	DQ ₆₀ *		
13	DQ ₄	33	A ₂	53	DQ ₁₅	73	NC	93	DQ ₂₀	113	V _{DD}	133	DQ ₂₉		
14	DQ ₃₆ *	34	A ₅	54	DQ ₄₇ *	74	CLK ₁	94	DQ ₅₂ *	114	V _{DD}	134	DQ ₆₁ *		
15	DQ ₅	35	V _{SS}	55	V _{SS}	75	V _{SS}	95	DQ ₂₁	115	DQMB ₂	135	DQ ₃₀		
16	DQ ₃₇ *	36	V _{SS}	56	V _{SS}	76	V _{SS}	96	DQ ₅₃ *	116	DQMB ₆ *	136	DQ ₆₂ *		
17	DQ ₆	37	DQ ₈	57	NC	77	NC	97	DQ ₂₂	117	DQMB ₃	137	DQ ₃₁		
18	DQ ₃₈ *	38	DQ ₄₀ *	58	NC	78	NC	98	DQ ₅₄ *	118	DQMB ₇ *	138	DQ ₆₃ *		
19	DQ ₇	39	DQ ₉	59	NC	79	NC	99	DQ ₂₃	119	V _{SS}	139	V _{SS}		
20	DQ ₃₉ *	40	DQ ₄₁ *	60	NC	80	NC	100	DQ ₅₅ *	120	V _{SS}	140	V _{SS}		

* Not used

(continued on the next page)

PIN CONFIGURATION *(continued)*

Pin Arrangement



Pin Functions

Pin Name	Pin Function
A0-A10/AP, A11-A12	Address Inputs (multiplexed)
BA0, BA1	Select Bank
DQ0-DQ31	Data In/Out
\overline{WE}	Read/Write Enable
CLK0, CLK1	Clock Input
CKE0	Clock Enable Input
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
DQMB0-DQMB3	Data Input/Output Mask
$\overline{S_0}$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

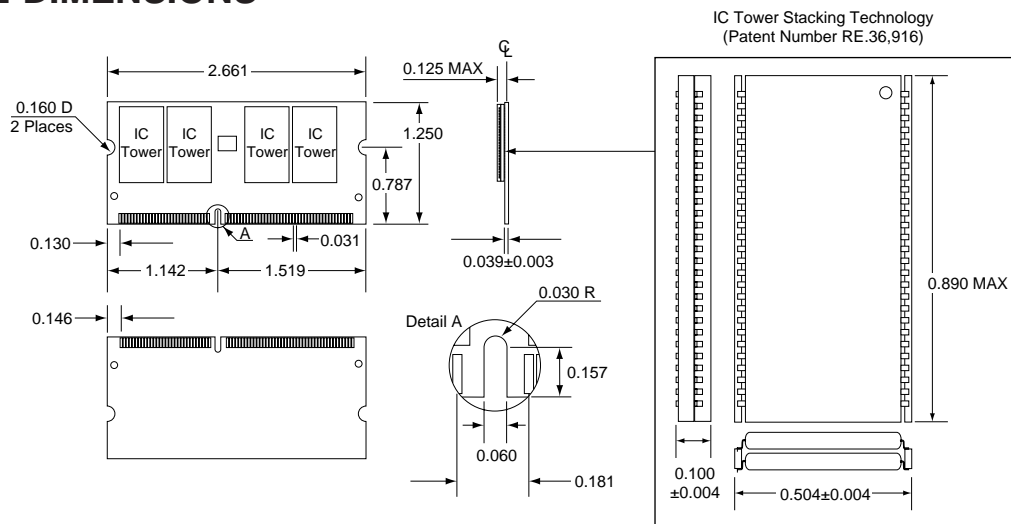
ORDERING INFORMATION

Part Number	PC100 100MHz Parameters					
	CL	tRCD	tRP	tRC	Units	Comment
N/A	3	3	3	8	clks	slowest supported (option "A")
N/A	3	2	3	8	clks	2nd choice (option "B")
SL32G8P64M8G-A10CVU	3	2	2	7	clks	target (option "C")
SL32G8P64M8G-A10DVU	2	2	2	7	clks	goal (option "D")

Note: The "U" suffix added to the part number selects the RoHS compliant lead-free version.

PACKAGE DIMENSIONS

Units: Inches



816-1

TOLERANCES: ± 0.005 UNLESS OTHERWISE SPECIFIED

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I²C; Current sink capability of SDA driver ≤3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported				Hex Value			
		A	B	C	D	A	B	C	D
0	# of bytes written into serial memory at module manufacturer	128 bytes				80h			
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)				08h			
2	Fundamental memory type	SDRAM				04h			
3	# of row addresses on this assembly	13				0Dh			
4	# of column addresses on this assembly	11				0Bh			
5	# of module banks on this assembly	1 bank				01h			
6	Data width of this assembly	32 bits				20h			
7	...Data width of this assembly (continued)	—				00h			
8	Voltage interface standard of this assembly	LVTTL				01h			
9	SDRAM cycle time at CL=3 (t _{CYC})	—	—	10ns	10ns	—	—	A0h	A0h
10	SDRAM access time from clock at CL=3 (t _{AC})	—	—	6ns	6ns	—	—	60h	60h
11	DIMM configuration type	None				00h			
12	Refresh rate/type	7.8μs, Self-refresh				82h			
13	SDRAM width	4 bits				04h			
14	Error Checking DRAM data width	0 bits				00h			
15	Min. CLK delay for back-to-back rand. col. addr.	t _{CCD} =1 CLK				01h			
16	SDRAM device attributes: burst lengths supported	1,2,4 and 8				0Fh			
17	SDRAM device attributes: # of banks on SDRAM device	4 banks				04h			
18	SDRAM device attributes: CAS latency	CAS latency = 2,3				06h			
19	SDRAM device attributes: CS latency	CS latency = 0				01h			
20	SDRAM device attributes: Write latency	Write Latency = 0				01h			
21	SDRAM module attributes	non-buff., non-reg.				00h			
22	SDRAM device attributes: general	V _{CC} 10%, B/R, S/W, P/A, A/P				0Eh			
23	Minimum clock cycle time at CL=2 (t _{CYC})	—	—	15ns	10ns	—	—	F0h	A0h
24	Max. data access time form clock at CL=2 (t _{AC})	—	—	8ns	6ns	—	—	80h	60h
25	Minimum clock cycle time at CL=1 (t _{CYC})	—	—	—	—	—	—	00h	00h
26	Max. data access time from clock at CL=1 (t _{AC})	—	—	—	—	—	—	00h	00h
27	Minimum row precharge time (t _{RP})	—	—	20ns	20ns	—	—	14h	14h
28	Minimum row active to row active delay (t _{RRD})	—	—	20ns	20ns	—	—	14h	14h
29	Minumum RAS to CAS (t _{RCD})	—	—	20ns	20ns	—	—	14h	14h
30	Minumum RAS pulse width (t _{RAS})	—	—	50ns	50ns	—	—	32h	32h
31	Module bank density	256MB				40h			
32	Min. command and address signal setup time (t _{AS})	2ns				20h			
33	Min. command and address signal hold time (t _{AH})	1ns				10h			
34	Min. data signal input setup time (t _{DS})	2ns				20h			

continued on the next page

Byte #	Function Described	Function Supported				Hex Value			
		A	B	C	D	A	B	C	D
35	Min. data signal input hold time (t _{DH})	1ns				10h			
36-61	Superset information (may be used in future)	—				00h			
62	SPD revision	—	—	1.2	1.2	—	—	12h	12h
63	Checksum for bytes 0-62	JEDEC calculation				xxh			
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code				7Fh			
65	Man. JEDEC ID code (continued)	STEC's ID				A8h			
66-71						00h			
72	Manufacturing location	STEC USA or STEC Malaysia				01h (USA) or 02h			
73-90	Manufacturer's part number					xxh			
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)				01h			
92						00h			
93	Manufacturing date	Year (BCD)				yy			
94		Calender Week (BCD)				w w			
95	Assembly serial number	Tester number				ss			
96		Serial number (bits 7-0)				ss			
97		Serial number (bits 15-8)				ss			
98		Serial number (bits 23-16)				ss			
99-125	Manufacturer's specific data					xxh			
126	Intel specification frequency	100MHz				64h			
127	Intel specification details	Detailed 100MHz Info				—	—	CFh	CFh

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to VSS	VIN, VOUT	-1.0 to +4.6	V
Voltage on VCC Supply Relative to VSS	VDD	-1.0 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	PD	8	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to VSS, TA=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	0	0.8	V	2
Output High Voltage Level	V _{OH}	2.4	—	—	V	I _{OH} =-2mA
Output Low Voltage Level	V _{OL}	—	—	0.4	V	I _{OL} =2mA
Input Leakage Current	I _{IL}	-80	—	80	μA	3
Output Leakage Current	I _{OL}	-10	—	10	μA	4

Notes:

1. V_{IH}(max)=5.6 V AC (pulse width <=3 ns acceptable)
2. V_{IL}(min) = -2.0 V AC (pulse width <=3 ns acceptable)
3. Any input 0<=V_{IN}<=V_{DD}+0.3V, all other pins not under test = 0 V.
4. Data out is disabled, 0<=V_{OUT}<=V_{DD}

CAPACITANCE (TA=23 °C, f=1MHz)

Item	Symbol	Max	Units
Input Capacitance (A ₀ -A ₁₀ /AP, A ₁₁ - ₁₂ , BA ₀ , BA ₁)	C _{IN1}	50	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{WE})	C _{IN2}	50	pF
Input Capacitance (CLK ₀ , CLK ₁)	C _{IN3}	21	pF
Input Capacitance (CKE ₀)	C _{IN4}	50	pF
Input Capacitance ($\overline{S_0}$)	C _{IN5}	50	pF
Input Capacitance (DQMB ₀ -DQMB ₃)	C _{IN6}	20	pF
Input/Output Capacitance (DQ ₀ -DQ ₃₁)	C _{IO1}	16.5	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted. TA=0 to 70°C)

Parameter	Symbol	Test Condition	Max	Units
Operating Current (One Bank Active)	ICC1S	Burst length=1, tRC>=tRC(min), IOL=0mA, Outputs open	880	mA
Precharge Standby Current in Power-Down Mode	ICC2P	CKE<=VIL(max), tCLK=10ns,	16	mA
	ICC2PS	CKE and CLK<=VIL(max), tCLK=infinity	16	mA
Precharge Standby Current in Non Power-Down Mode	ICC2N	CKE and S>=VIH(min), tCLK=10ns Input signals are changed one time during 20ns	128	mA
	ICC2NS	CKE>=VIH(min), CLK<=VIL(max), tCLK=infinity Input signals are stable	112	mA
Active Standby Current in Power-Down Mode	ICC3P	CKE<=VIL(max), tCLK=10ns	48	mA
	ICC3PS	CKE and CLK<=VIL(max), tCLK=infinity	48	mA
Active Standby Current in Non Power-Down Mode (One Bank Active)	ICC3N	CKE and S>=VIH(min), tCLK=10ns, Input signals are changed one time during 20ns	240	mA
	ICC3NS	CKE>=VIH(min), CLK<=VIL(max), tCLK=infinity Inputs are stable	200	mA
Operating Current (Burst Mode)	ICC4	IOL=0mA, Page Burst, ICCD=2 CLKs, Outputs open 4 banks activated	920	mA
Refresh Current (Refresh Period is 64ms)	ICC5	tRC>=tRC(min)	1680	mA
Self Refresh Current	ICC6	CKE<=0.2V	24	mA

AC TIMING PARAMETERS

(AC operating conditions unless otherwise noted. Refer to the individual component, not the whole module.)

Parameter	Symbol	Min	Max	Unit	Notes
Clock Period	CL=2 CL=3	tCYC	15/10*	ns	
Clock High Time		tCH	3	ns	1
Clock Low Time		tCL	3	ns	
Input Setup Times		tSI	2	ns	
Input Hold Times		tHI	1	ns	
Output Valid From Clock	CL=2 CL=3	tAC		8/6* 6	2 3
Output Hold From Clock		tOH	3	ns	4
Output Valid to Z		tOHZ	3	9	ns
CAS to CAS Delay		tCCD	1		tCLK
CAS Bank Delay		tCBD	1		tCLK
CKE to Clock Disable		tCKE	1		tCLK
RAS Precharge Time		tRP	2		tCLK
RAS Active Time		tRAS	5		tCLK
Active to Command Delay (RAS to CAS Delay)		tRCD	2		tCLK
RAS to RAS Bank Activate Delay		tRRD	2		tCLK
RAS Cycle Time		tRC	7		tCLK
DQM to Input Data Delay		tDQD	0		tCLK
Write Cmd. to Input Data Delay		tDWD	0		tCLK
Mode Register set to Active Delay		tMRD	3		tCLK
Precharge to O/P in High-Z		tROH	CL		tCLK
DQM to Data in HiZ for Read		tDQZ	2		tCLK
DQM to Data Mask for Write		tDQM	0		tCLK
Data-In to PRE Command Period		tDPL	2		tCLK
Data-In to ACT (PRE) Command Period (Auto Precharge)		tDAL	5		tCLK
Power Down Mode Entry		tSB		1	tCLK
Self Refresh Exit Time		tSRX	1		tCLK
Power Down Exit Setup Time		tPDE	1		tCLK
Clock Stop During Self Refresh or Power Down		tCLKSTP	200		tCLK

* These values depend on the PC100 option. The first value is for PC100 Option C and the second value is for PC100 Option D.

AC TIMING PARAMETERS (continued)

Notes:

1. Rated @ 1.5V
2. Limited application, 2 banks, all outputs switching
3. LVTTTL levels, rated @ 50pF, all outputs switching, 5.2ns @ 0pF
4. 3ns @ 50pF, need 1.8ns @0pF
5. $t_{RP}=2$ a SPD Option
6. $t_{RCD}=2$ a SPD Option
7. 7 clks for $t_{RP}=2$
8. Data Masked on the same clock.
9. Timing is asynchronous. If t_{SET} is not met by rising edge of CLK then CKE is assumed latched on next cycle.
10. If the clock is stopped during self refresh or powerdown, 200 clocks are required before CKE is high.

AC OPERATING TEST CONDITIONS

($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value
AC input levels	$V_{IH}/V_{IL}=2.4V/0.4V$
Input timing measurement ref. level	1.4V
Input rise and fall time	$t_r/t_f=1ns/1ns$
Output measurement reference level	1.4V
Output load condition	See Figure 2.

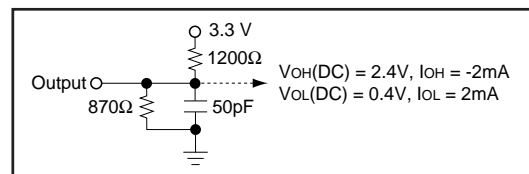


Figure 1. DC Output Load Circuit

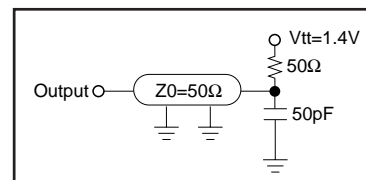


Figure 2. AC Output Load Circuit

REVISION HISTORY

Rev. **Change Description from Previous Revision**

-102 08/07/2007. Logo updated.

-103 08/24/2007. U added to part number.