

256M X 72 Bit (2GB) 168-Pin Registered SDRAM DIMM ECC (PC133) 2 Rank x 4

FEATURES

- PC133 Compliant
(Option A: $t_{CYC} = 7.5ns@CL = 3$)
(Option D: $t_{CYC} = 7.5ns@CL = 2, 3$)
- Burst Mode Operation
- Auto and self refresh capability
(8192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V \pm 0.3V power supply
- MRS cycle with address key programs
 - CAS Latency (CL = 2 or 3)
 - Burst Length (1, 2, 4, 8, and Full Page)
 - Data Type (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with 256 Byte EEPROM
- ECC
- RoHS Compliant and Industrial Operating Temperature versions available

GENERAL DESCRIPTION

The SL72R5M256M8H-A75xV(W)(U) is a 256M x 72 bit Synchronous Dynamic RAM (SDRAM) 168-pin Registered Dual In-line Memory Module (RDIMM) with ECC.

This module consists of thirty-six CMOS 32M x 4 bit x 4 bank SDRAMs in 54-pin 400-mil TSOP-II packages mounted in stacks of two on a 168-pin glass epoxy substrate using the patented IC Tower stacking technology (Patent Number RE.36,916). The SDRAMs are organized in 2 ranks.

A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors are mounted in parallel across the power supply. Damping resistors are added in series on the data signals. PLL circuits supply clocks to the SDRAMs from one clock input.

All control and address signals are re-driven through three registers to the SDRAM devices. The control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock).

The module has gold edge connections and is intended for mounting into 168-pin DIMM edge connector sockets keyed for 3.3V power supply. The module is PC133 compliant.

ORDERING INFORMATION

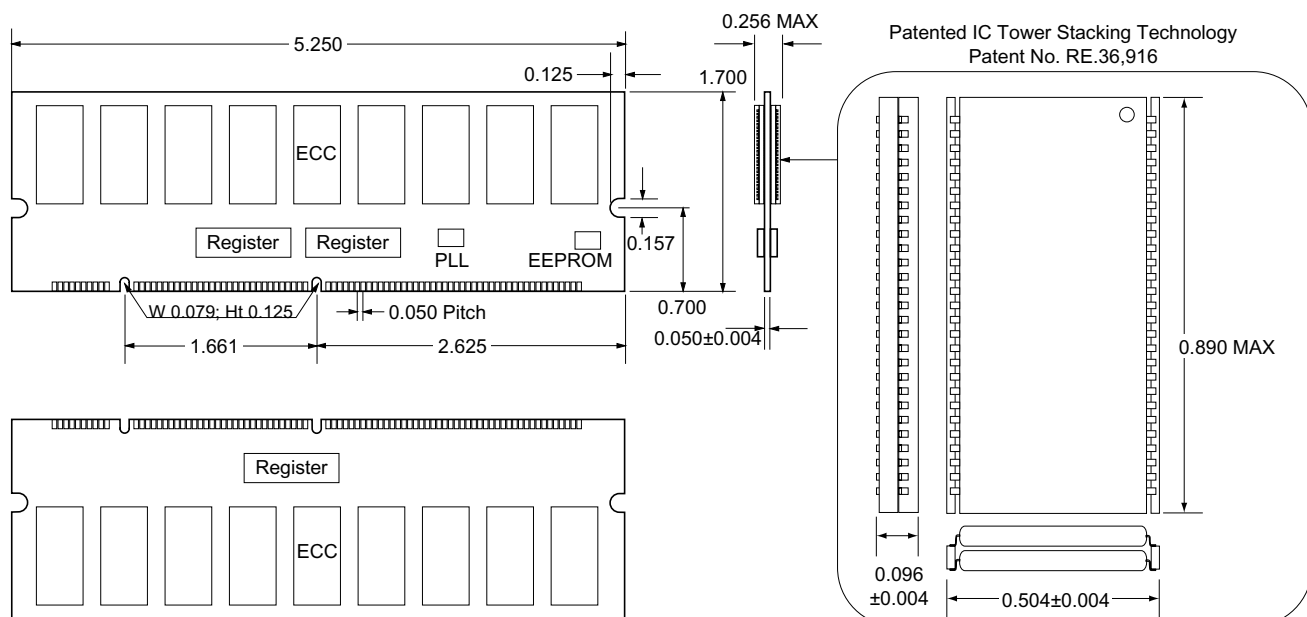
Part Number	t _{CYC}	CL	t _{RCD}	t _{RP}	t _{RC}	Comment
SL72R5M256M8H-A75AV(W)(U)	7.5ns	3clks	20ns	20ns	66ns	Refer to option A in this specification.
SL72R5M256M8H-A75DV(W)(U)	7.5ns	2clks	15ns	15ns	60ns	Refer to option D in this specification.

Notes:

1. A "W" in the suffix of the part number selects the Industrial Operating Temperature Range version of the module (T_A = -40 to 85°C). This version is built with Industrial Temperature SDRAMs.
2. The "U" in the part number selects the RoHS Compliant, lead-free version of the module.

PACKAGE DIMENSIONS

Units are in inches. Tolerances are ± 0.005 unless otherwise specified.



(Where x selects PC133 CAS Latency; W = Industrial Operating Temperature; U = RoHS Compliant, lead-free version.)

PIN CONFIGURATION

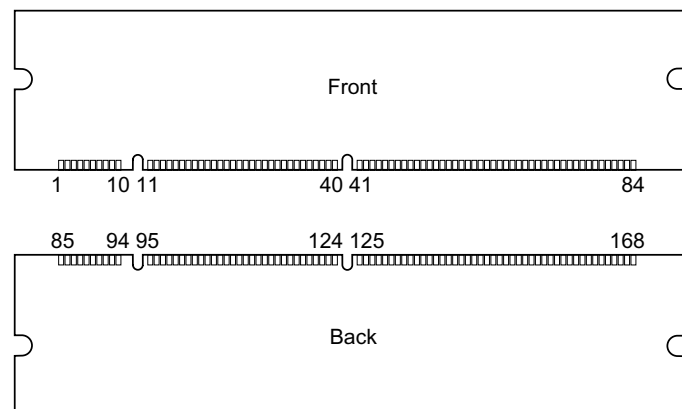
Pin Symbols (* = Not Used)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	25	NC	49	VDD	73	VDD	97	DQ41	121	A9	145	NC		
2	DQ0	26	VDD	50	NC	74	DQ28	98	DQ42	122	BA0	146	NC		
3	DQ1	27	\overline{WE}	51	NC	75	DQ29	99	DQ43	123	A11	147	REGE		
4	DQ2	28	DQMB0	52	CB2	76	DQ30	100	DQ44	124	VDD	148	VSS		
5	DQ3	29	DQMB1	53	CB3	77	DQ31	101	DQ45	125	CLK1	149	DQ53		
6	VDD	30	\overline{S}_0	54	VSS	78	VSS	102	VDD	126	A12	150	DQ54		
7	DQ4	31	NC	55	DQ16	79	CLK2	103	DQ46	127	VSS	151	DQ55		
8	DQ5	32	VSS	56	DQ17	80	NC	104	DQ47	128	CKE0	152	VSS		
9	DQ6	33	A0	57	DQ18	81	NC	105	CB4	129	\overline{S}_3	153	DQ56		
10	DQ7	34	A2	58	DQ19	82	SDA	106	CB5	130	DQMB6	154	DQ57		
11	DQ8	35	A4	59	VDD	83	SCL	107	VSS	131	DQMB7	155	DQ58		
12	VSS	36	A6	60	DQ20	84	VDD	108	NC	132	A13*	156	DQ59		
13	DQ9	37	A8	61	NC	85	VSS	109	NC	133	VDD	157	VDD		
14	DQ10	38	A10/AP	62	NC	86	DQ32	110	VDD	134	NC	158	DQ60		
15	DQ11	39	BA1	63	CKE1	87	DQ33	111	\overline{CAS}	135	NC	159	DQ61		
16	DQ12	40	VDD	64	VSS	88	DQ34	112	DQMB4	136	CB6	160	DQ62		
17	DQ13	41	VDD	65	DQ21	89	DQ35	113	DQMB5	137	CB7	161	DQ63		
18	VDD	42	CLK0	66	DQ22	90	VDD	114	\overline{S}_1	138	VSS	162	VSS		
19	DQ14	43	VSS	67	DQ23	91	DQ36	115	\overline{RAS}	139	DQ48	163	CLK3		
20	DQ15	44	NC	68	VSS	92	DQ37	116	VSS	140	DQ49	164	NC		
21	CB0	45	\overline{S}_2	69	DQ24	93	DQ38	117	A1	141	DQ50	165	SA0		
22	CB1	46	DQMB2	70	DQ25	94	DQ39	118	A3	142	DQ51	166	SA1		
23	VSS	47	DQMB3	71	DQ26	95	DQ40	119	A5	143	VDD	167	SA2		
24	NC	48	NC	72	DQ27	96	VSS	120	A7	144	DQ52	168	VDD		

Pin Functions

Pin Symbol	Pin Function
A0-A9, A11, A12	Address Inputs
A10/AP	Address/Autoprecharge
BA0, BA1	SDRAM Bank Address
DQ0-DQ63	Data Inputs/Outputs
CB0-CB7	Check Bits Inputs/Outputs
\overline{WE}	Write Enable
CLK0	Clock Inputs
CKE0, CKE1	Clock Enables
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
DQMB0-DQMB7	Data Mask
\overline{S}_0 - \overline{S}_3	Chip Selects
REGE	Register Enable
SDA	SPD Data Input/Output
SCL	SPD Clock Input
SA0-SA2	SPD Address Input
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

Pin Locations

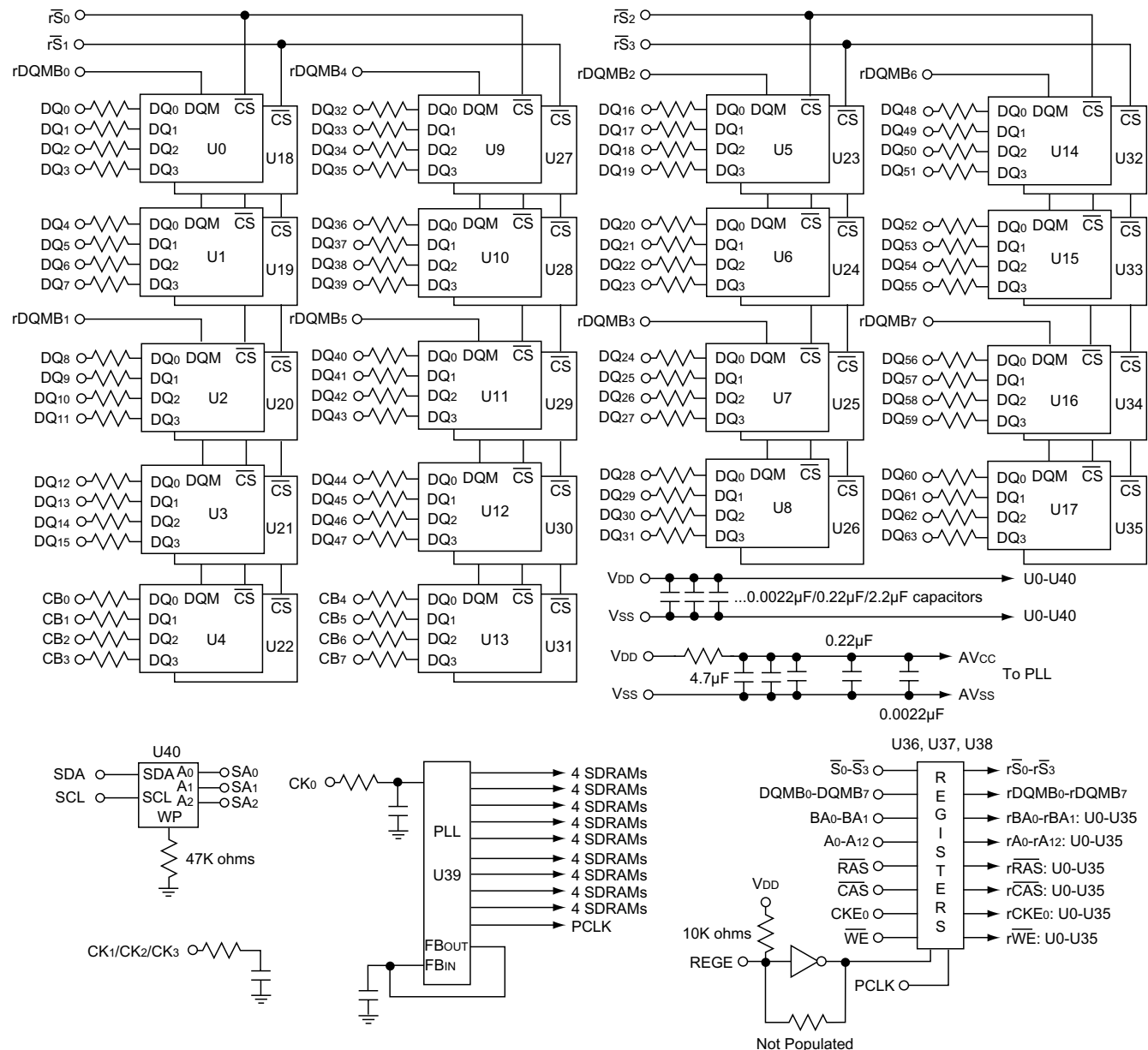


SL72R5M256M8H-A75xV(W)(U)

168-PIN DIMM

(Where x selects PC133 CAS Latency; W = Industrial Operating Temperature; U = RoHS Compliant, lead-free version.)

FUNCTIONAL BLOCK DIAGRAM



- Notes:
1. All resistors are 10 ohms unless otherwise specified.
 2. DQ wiring may differ from that described in this drawing; however, DQ/DQMB relationships are maintained as shown.

SERIAL PRESENCE DETECTS

Serial PD Interface Protocol: I²C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
0	# of bytes written into serial memory at module manufacturer	128 bytes		80h	
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)		08h	
2	Fundamental memory type	SDRAM		04h	
3	# of row addresses on this assembly	13		0Dh	
4	# of column addresses on this assembly	12		0Ch	
5	# of module ranks on this assembly	2 ranks		02h	
6	Data width of this assembly	72 bits		48h	
7	...Data width of this assembly (continued)	—		00h	
8	Voltage interface standard of this assembly	LVTTTL		01h	
9	SDRAM cycle time at CL=3 (tCYC)	7.5ns	7.5ns	75h	75h
10	SDRAM access time from clock at CL=3 (tAC)	5.4ns	5.4ns	54h	54h
11	DIMM configuration type	ECC		02h	
12	Refresh rate/type	7.8µs, Self-refresh		82h	
13	SDRAM width	4 bits		04h	
14	Error Checking DRAM data width	4 bits		04h	
15	Min. CLK delay for back-to-back rand. col. addr.	tCCD=1 CLK		01h	
16	SDRAM device attributes: burst lengths supported	1,2,4,8, and Full Page		8Fh	
17	SDRAM device attributes: # of banks on SDRAM device	4 banks		04h	
18	SDRAM device attributes: CAS latency	CAS latency = 2,3		06h	
19	SDRAM device attributes: CS latency	CS latency = 0		01h	
20	SDRAM device attributes: Write latency	Write Latency = 0		01h	
21	SDRAM module attributes	Registered/Buffered/PLL		1Fh	
22	SDRAM device attributes: general	V _{CC} 10%, B/R, S/W, P/A, A/P		0Eh	
23	Minimum clock cycle time at CL=2 (tCYC)	10ns	75ns	A0h	75h
24	Max. data access time form clock at CL=2 (tAC)	6ns	5.4ns	60h	54h
25	Minimum clock cycle time at CL=1 (tCYC)	—	—	00h	00h
26	Max. data access time from clock at CL=1 (tAC)	—	—	00h	00h
27	Minimum row precharge time (tRP)	20ns	15ns	14h	0Fh
28	Minimum row active to row active delay (tRRD)	15ns	15ns	0Fh	0Fh
29	Minumum RAS to CAS (tRCD)	20ns	15ns	14h	0Fh
30	Minumum RAS pulse width (tRAS)	45ns	45ns	2Dh	2Dh
31	Module bank density	1GB		01h	
32	Min. command and address signal setup time (tAS)	1.5ns		15h	
33	Min. command and address signal hold time (tAH)	0.8ns		08h	
34	Min. data signal input setup time (tDS)	1.5ns		15h	
35	Min. data signal input hold time (tDH)	0.8ns		08h	
36-61	Superset information (may be used in future)	—		00h	
62	SPD revision	JEDEC 2		02h	
63	Checksum for bytes 0-62	JEDEC calc		xxh	
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code		7Fh	
65	Man. JEDEC ID code (continued)	STEC's ID		A8h	

continued on the next page

(Where x selects PC133 CAS Latency; W = Industrial Operating Temperature; U = RoHS Compliant, lead-free version.)

SERIAL PRESENCE DETECTS *(continued)*

Byte #	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
66-71	—	—		00h	
72	Manufacturing location	STEC USA/Malaysia		01h/02h	
73-90	Manufacturer's part number			xxh	
91	PCB Revision code	RevA(01), RevB(02)		xxh	
92	—	—		00h	
93	Manufacturing date	Year(BCD format)		yyh	
94	—	Calender Week(BCD format)		w w h	
95	Assembly serial number	Tester Number		ssh	
96	—	serial#(bits7-0)		ssh	
97	—	serial#(bits15-8)		ssh	
98	—	serial#(bits23-16)		ssh	
99-125	Manufacturer's specific data			xxh	
126	Intel specification frequency	100MHz		64h	
127	Intel specification details	CLK0; junc temp.TBD; CL2,CL3; concurrent AP		8Fh	
128+	—			00h	

ABSOLUTE MAXIMUM RATINGS¹

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to VSS	V _{IN} , V _{OUT}	-1.0 to +4.6	V
Voltage on VCC Supply Relative to VSS	V _{DD}	-1.0 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	36	W
Short Circuit Output Current	I _{OS}	50	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to VSS=0)

Item	Symbol	Min	Typ	Max	Unit	Notes
Commercial Operating Temperature Range	T _A	0	25	70	°C	
Industrial Operating Temperature Range	T _A	-40		85	°C	
Supply Voltage	V _{DD}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	0	0.8	V	2
Output High Voltage Level	V _{OH}	2.4	—	—	V	I _{OH} =-4mA
Output Low Voltage Level	V _{OL}	—	—	0.4	V	I _{OL} =4mA
Input Leakage Current	I _{IL}	-5	—	5	μA	3
Output Leakage Current	I _{OL}	-10		10		3, 4

- V_{IH}(max)=5.6 V AC (pulse width <=3 ns acceptable).
- V_{IL}(min) = -2.0 V AC (pulse width <=3 ns acceptable).
- Any input 0<=V_{IN}<=V_{DD}.
- Data out is disabled, 0<=V_{OUT}<=V_{DD}.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz, V_{REF}=1.4±200mA)

Item	Symbol	Max	Units
Input Capacitance (A, BA, RAS, CAS, WE) 5pF adder for board.	C _{IN1}	8.5	pF
Input Capacitance (CKE, S) 5pF adder for board.	C _{IN3}	8.5	pF
Input Capacitance (CLK) 5pF adder for board.	C _{IN2}	7.5	pF
Input Capacitance (DQMB) 5pF adder for board.	C _{IN4}	8.5	pF
Input/Output Capacitance (DQ) 5pF adder for board.	C _{IO1}	17	pF

DC CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Parameter/Condition	Symbol	Option D (Max)	Option A (Max)	Units	Notes
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; tRC >= tRC (MIN)	IDD1	2,223	2,043	mA	1,3,4,5,6
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW	IDD2	126	126	mA	5
STANDBY CURRENT: Active Mode; CKE = HIGH; \overline{CS} = HIGH; All banks active after tRCD met; No accesses in progress	IDD3	1,620	1,620	mA	1,2,4,5,6
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active	IDD4	2,313	2,133	mA	1,3,4,5,6
AUTO REFRESH CURRENT: tRFC = tRFC (MIN) CKE = HIGH; \overline{CS} = HIGH	IDD5	4,653	4,653	mA	1,2,3,4,5,6
SELF REFRESH CURRENT: Standard CKE <= 0.2V	IDD7	216	216	mA	

1. IDD is dependent on output loading and cycle rates.
Specified values are obtained with minimum cycle time and the outputs open.
2. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
3. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. For Option D, CL=2 and tCK=7.5ns. For Option A, CL=3 and tCK=7.5ns.
6. For modules with more than one rank, IDDN is specified with one rank in IDDN and the other ranks in IDD2, where n is IDD number in the Symbol column.

AC TIMING PARAMETERS (Recommended operating conditions unless otherwise specified.)

Parameter	Symbol	Option A		Option D		Unit	Notes
		Min	Max	Min	Max		
Clock Period	CL3	tCLK	7.5		7.5		ns
	CL2		10		7.5		ns
Clock High Time (Rated @1.5V)		tCH	2.5		2.5		ns
Clock Low Time		tCL	2.5		2.5		ns
Input Setup Times (Data) (Address/Command & CKE)		tSI	1.5		1.5		ns
			1.5		1.5		
Input Hold Times (Data) (Address/Command & CKE)		tHI	0.8		0.8		ns
			0.8		0.8		
Output Valid From Clock (LVTTL levels; Rated@50pF; all outputsswitching)	CL3	tAC		5.4		5.4	ns
	CL2			6		5.4	ns
Output Hold From Clock (Rated@50pF)		tOH	2.7		2.7		ns
CAS to CAS Delay		tCCD	1		1		tCLK
CKE to Clock Disable		tCKE	1		1		tCLK
RAS Precharge Time		tRP	20		15		ns
RAS Active Time		tRAS	45	120K	45	120K	ns
Active to Command Delay (RAS to CAS Delay)		tRCD	20		15		ns
RAS to RAS Bank Activate Delay		tRRD	15		15		ns
RAS Cycle Time		tRC	66		60		ns
DQM to Input Data Delay		tDQD	0		0		tCLK
Write Cmd. to Input Data Delay		tDWD	0		0		tCLK
Mode Register Set to Active Delay		tMRD	2		2		tCLK
Precharge to O/P in High-Z		tROH		CL		CL	tCLK
DQM to Data in Hi-Z for Read		tDQZ	2		2		tCLK
DQM to Data Mask for Write		tDQM	0		0		tCLK
Data-In to PRE Command Period		tDPL	2		2		tCLK
Data-In to ACT (PRE) Cmd Period (Auto Precharge)		tDAL	4		5		tCLK
Power Down Mode Entry		tSB		1		1	tCLK
Exti Self Refresh to Active Time		tXSR	75		67		ns
Power Down Exit Set Up Time		tPDE	1		1		tCLK
Clock Stop During Self Refresh or Power Down		tCLKSTP	200		200		tCLK
Refresh Period		tREF		64		64	ms

Notes:

- Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V. tACN=access time with 0pF load.
- CL=CAS Latency.
- Data Masked on the same clock.
- Timing is asynchronous. If tset is not met by rising edge of CLK then CKE is assumed latched on next cycle.
- If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
- For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit and 512Mbit technology, 8192 refresh cycles.

REVISION HISTORY

Rev. Change Description from Previous Revision

- 102 10/30/2006. Updated to latest format and die revs.
- 103 08/13/2007. Updated logo, web address and SPD.

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