



SL72A8M64M8M-A06EW(W)(U)

(Where second W selects Industrial Operating Temperature; U selects RoHS Compliant, lead-free version.)

64M X 72 Bit (512MB) 200-Pin DDR SDRAM SO-DIMM with ECC (PC2700) 1 Rank x 8

FEATURES

- PC2700 Compliant (DDR333B 167MHz-6ns@CL = 2.5)
- 200-Pin SO-DIMM form factor
- Auto and self refresh capability (8192 cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- +2.5V ± 0.2V VDD
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- Serial Presence Detect with EEPROM
- ECC
- RoHS Compliant, lead-free version available
- Commercial and Industrial Operating Temperature ranges available

GENERAL DESCRIPTION

The SL72A8M64M8M-A06EW(W)(U) is a 64M x 72 bit Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) 200-pin Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of nine CMOS 16M x 8 bit x 4 bank DDR SDRAMs in 66-pin 400-mil TSOP II packages mounted on a 200-pin glass epoxy substrate.

A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors are mounted in parallel across the power supply. Damping resistors are mounted in series on the DQ, DQS, and DM signals. A PLL supplies clocks to the SDRAMs from one clock input.

The module has gold edge connections and is intended for mounting into 200-pin SO-DIMM edge connector sockets keyed for 2.5V.

ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72A8M64M8M-A06EW(W)(U)	2.5	166	2.7 GB/s

Notes:

1. The Operating Temperature Range is selected as follows:
Commercial (0 to 70°C): no additional designator in the part number; *Industrial (-40 to 85°C):* the second "W" is added to the part number.
2. The "U" suffix added to the part number selects RoHS Compliant, lead-free module.

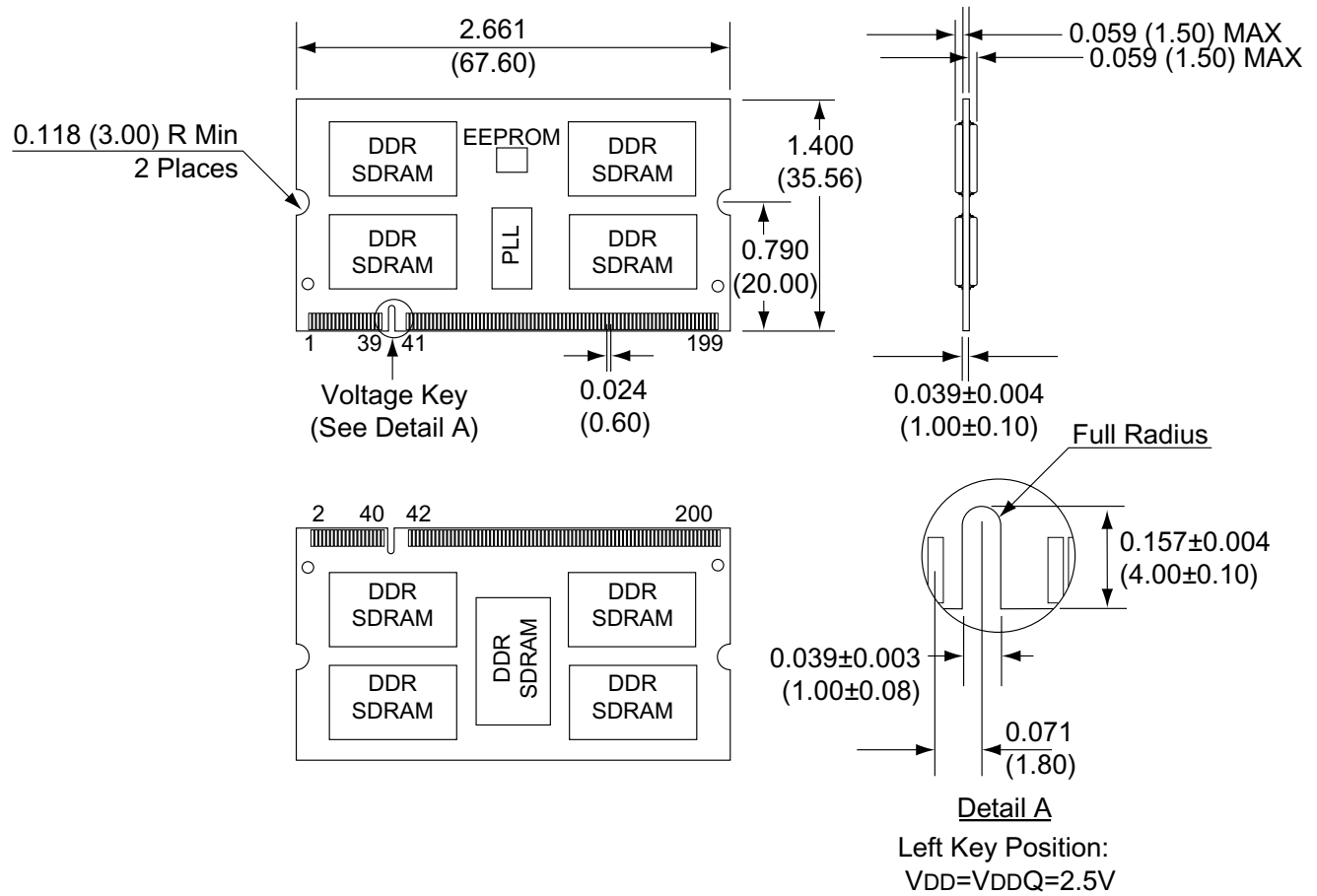
SL72A8M64M8M-A06EW(W)(U)

200-PIN SO-DIMM

(Where second W selects Industrial Operating Temperature; U selects RoHS Compliant, lead-free version.)

PACKAGE DIMENSIONS

Units are in inches (millimeters). Tolerances are ± 0.005 (± 0.127) unless otherwise specified.



(Where second W selects Industrial Operating Temperature; U selects RoHS Compliant, lead-free version.)

PIN CONFIGURATION (* = Not Used; / = Active Low)

Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	2	VREF	51	VSS	52	VSS	101	A9	102	A8	151	DQ42	152	DQ46
3	VSS	4	VSS	53	DQ19	54	DQ23	103	VSS	104	VSS	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	VDD	156	VDD
7	DQ1	8	DQ5	57	VDD	58	VDD	107	A5	108	A4	157	VDD	158	/CK1*
9	VDD	10	VDD	59	DQ25	60	DQ29	109	A3	110	A2	159	VSS	160	CK1*
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	VSS	162	VSS
13	DQ2	14	DQ6	63	VSS	64	VSS	113	VDD	114	VDD	163	DQ48	164	DQ52
15	VSS	16	VSS	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	/RAS	167	VDD	168	VDD
19	DQ8	20	DQ12	69	VDD	70	VDD	119	/WE	120	/CAS	169	DQS6	170	DM6
21	VDD	22	VDD	71	CB0	72	CB4	121	/S0	122	/S1*	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	A13*	124	BA2*	173	VSS	174	VSS
25	DQS1	26	DM1	75	VSS	76	VSS	125	VSS	126	VSS	175	DQ51	176	DQ55
27	VSS	28	VSS	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	VDD	180	VDD
31	DQ11	32	DQ15	81	VDD	82	VDD	131	VDD	132	VDD	181	DQ57	182	DQ61
33	VDD	34	VDD	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	VDD	85	DU	86	/RESET*	135	DQ34	136	DQ38	185	VSS	186	VSS
37	/CK0	38	VSS	87	VSS	88	VSS	137	VSS	138	VSS	187	DQ58	188	DQ62
39	VSS	40	VSS	89	CK2*	90	VSS	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	/CK2*	92	VDD	141	DQ40	142	DQ44	191	VDD	192	VDD
43	DQ17	44	DQ21	93	VDD	94	VDD	143	VDD	144	VDD	193	SDA	194	SA0
45	VDD	46	VDD	95	CKE1*	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	VDDSPD	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	VSS	150	VSS	199	VDDID	200	DU

Pin Description

Pin Symbol	Pin Function
CK0	Clock inputs, positive line
/CK0	Clock inputs, negative line
CKE0	Clock enables
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
/S0	Chip selects
A(0:9,11,12)	Address inputs
A10/AP	Address input/Autoprecharge
BA(0:1)	SDRAM bank address
SCL	SPD clock input
SDA	SPD data input/output
SA(0:2)	SPD address

Pin Symbol	Pin Function
DQ(0:63)	Data input/output
CB(0:7)	Data check bits input/output
DM(0:8)	Data masks
DQS(0:8)	Data strobes
VDD	Core power (2.5V)
VSS	Ground
VREF	Input/output reference
VDDSPD	SPD power (2.2V to 5.5V)
VDDID	VDD identification flag (No connect for VDD=VDDQ)

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: IIC; Current sink capability of SDA driver $\leq 3\text{mA}$; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	DDR SDRAM	07h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	11	0Bh
5	# of physical ranks on this assembly	1 rank	01h
6	Data width of this assembly	72 bits	48h
7	...Data width of this assembly (continued)	—	00h
8	Voltage interface level of this assembly	SSTL 2.5V	04h
9	SDRAM cycle time at CL=3 (tCYC)	6ns	60h
10	SDRAM access time from clock at CL=3 (tAC)	0.7ns	70h
11	DIMM configuration type	ECC	02h
12	Refresh rate/type	7.8 μs , Self -refresh	82h
13	SDRAM width	8 bits	08h
14	Error Checking SDRAM data width	8 bits	08h
15	Min. CLK delay for back-to-back rand. col. addr.	tCCD=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	2,4,8	0Eh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5	0Ch
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 1	02h
21	SDRAM module attributes	Differential clock, PLL	24h
22	SDRAM device attributes: general	VDD $\pm 0.2\text{V}$	00h
23	Minimum clock cycle time at CL=2.5 (tCYC)	7.5ns	75h
24	Max. data access time form clock at CL=2.5 (tAC)	0.7ns	70h
25	Minimum clock cycle time at CL=2 (tCYC)	—	00h
26	Max. data access time from clock at CL=2 (tAC)	—	00h
27	Minimum row precharge time (tRP)	18ns	48h
28	Minimum row active to row active delay (tRRD)	12ns	30h
29	Minumum RAS to CAS (tRCD)	18ns	48h
30	Minumum RAS pulse width (tRAS)	42ns	2Ah
31	Module bank density	512MB	80h
32	Min. command and address signal setup time (tIS)	0.75ns	75h
33	Min. command and address signal hold time (tIH)	0.75ns	75h
34	Min. data/data mask signal input setup time (tDS)	0.45ns	45h
35	Min. data/data mask signal input hold time (tDH)	0.45ns	45h

continued on the next page

SERIAL PRESENCE DETECT INFORMATION (continued)

Byte #	Function Described	Function Supported	Hex Value
36-40	Reserved		00h
41	Row cycle time (trc)	60ns	3Ch
42	Auto refresh cycle time (trfc)	72ns	48h
43	Maximum SDRAM device cycle time (tCK_MAX)	13ns	34h
44	DQS-DQ skew (tdQSQ)	0.45ns	2Dh
45	SDRAM device data hold skew factor (tQHS)	0.60ns	60h
46	Reserved		00h
47	DDR SDRAM DIMM height	No Height Available	00h
48-61	Reserved		00h
62	SPD revision	JEDEC 1.0	00h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71			00h
72	Manufacturing location	STEC USA or STEC Malaysia	01h (USA) or 02h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	RevA(01),RevB(02)	xxh
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	w w
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-127	Manufacturer's specific data		xxh
128-255	Open for Customer Use	Undefined	00h

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional Operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time may affect device reliability.

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V _{IN} , V _{OUT}	-0.5 to +3.6	V
Voltage on VDD supply relative to VSS	V _{DD}	-1.0 to +3.6	V
Voltage on VDDQ supply relative to VSS	V _{DDQ}	-1.0 to 3.6	V
Storage temperature	T _{STG}	-55 to +150	°C
Power Dissipation	P _D	13.5	W
Short circuit current	I _{OS}	50	mA

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

Recommended operating conditions (Voltage referenced to VSS=0V)

Parameter	Symbol	Min	Max	Unit	Notes
<i>Operating Temperature</i>					
Commercial (without part number designator)	T _A	0	70	°C	
Industrial (with added part number designator, 2nd "W")	T _A	-40	85	°C	
Supply Voltage (for device with a nominal VDD of 2.5V)	V _{DD}	2.3	2.7	V	
I/O Supply voltage	V _{DDQ}	2.3	2.7	V	
I/O Reference voltage	V _{REF}	0.49*V _{DDQ}	0.51*V _{DDQ}	V	1
I/O Termination voltage (system)	V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage	V _{IH} (DC)	V _{REF} +0.15	V _{DDQ} +0.3	V	4
Input logic low voltage	V _{IL} (DC)	-0.3	V _{REF} -0.15	V	4
Input voltage level, CK and /CK	V _{IN} (DC)	-0.3	V _{DDQ} +0.3	V	
Input differential voltage, CK and /CK	V _{ID} (DC)	0.36	V _{DDQ} +0.6	V	3
<i>Input leakage current</i>					
A, BA, /RAS, /CAS, /WE, CKE, /S	I _L	-18	18	µA	
CK, /CK	I _L	-10	10	µA	
DM	I _L	-2	2	µA	
Output leakage current: DQ, CB, DQS	I _{OZ}	-5	5	µA	
Output high current (V _{OUT} = V _{DDQ} - 0.373V, minimum V _{REF} , minimum V _{TT})	I _{OH}	-16.8		mA	
Output low current (V _{OUT} = 0.373V, maximum V _{REF} , maximum V _{TT})	I _{OL}	16.8		mA	

- Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of ≤ 3nH.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
- The value of V_IX is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.
- These characteristics obey the SSTL-2 class II standards.

DC CHARACTERISTICS

- For IDD0, IDD1, IDD4R, IDD4W, IDD5, and IDD7:
In a module with more than one rank, IDDn is calculated with one rank in the IDDn and the other ranks in IDD2P.
For IDD2P, IDD2F, IDD3P, IDD3N, and IDD6:
All ranks in IDDn.
where n=corresponding IDD condition listed in Symbol column.
- Values shown for DDR2 SDRAM components only.
- Values will differ depending on DRAM parts used on the module.
- IDD values are calculated using worst case specifications of currently available DRAMs from different manufacturers.

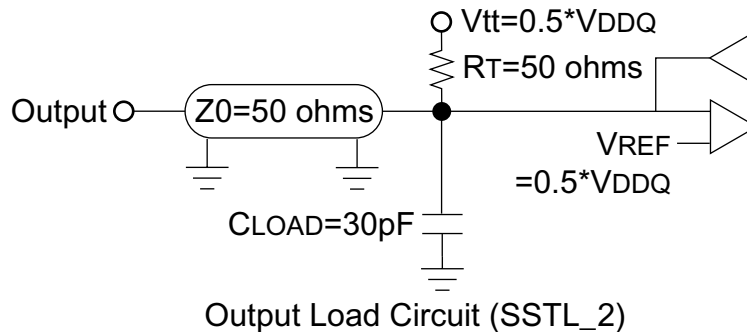
Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; t RC = t RC (MIN); t CK = t CK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;	IDD0	1,170	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; t RC = t RC (MIN); t CK = t CK (MIN); IOU = 0mA; Address and control inputs changing once per clock cycle	IDD1	1,440	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t CK = t CK (MIN); CKE = (LOW)	IDD2P	45	mA
IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; t CK = t CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	405	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t CK = t CK (MIN); CKE = LOW	IDD3P	315	mA
ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; t RC = t RAS (MAX); t CK = t CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	495	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); IOU = 0mA	IDD4R	1,665	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	1,665	mA
AUTO REFRESH CURRENT: t RC = t RC(MIN)	IDD5	2,610	mA
SELF REFRESH CURRENT: CKE <= 0.2V	IDD6	45	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, t RC = t RC (MIN); t CK = t CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7	3,645	mA

AC OPERATING CONDITIONS

(VDD=VDDQ=2.5V, Recommended Operating Temperature, f=1MHz)

Parameter/Condition	Symbol	Min	Max	Units	Note
Input High (Logic 1) Voltage, DQ, DQS, and DM signals	VIH(AC)	VREF+0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS, and DM signals	VIL(AC)		VREF-0.31	V	3
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relation to a Vref envelope that has been bandwidth limited 20MHz.



CAPACITANCE

(VDD=VDDQ=2.5V, TA=25°C, f=1MHz)

Parameter	Symbol	Max	Units
Input Capacitance : A, BA, /RAS, /CAS, /WE 20pF adder for board.	CIN0	47	pF
Input Capacitance : CKE, /S 20pF adder for board.	CIN1	47	pF
Input Capacitance: CK0, /CK0 5pF adder for board. PLL input.	CIN2	8	pF
Data and DQS I/O Capacitance: DQ, CB, DM, DQS 5 pF adder for board.	C/I/O	9	pF

(Where second W selects Industrial Operating Temperature; U selects RoHS Compliant, lead-free version.)

AC TIMING PARAMETERS (These AC characteristics were tested on the component.)

Symbol	Parameter	Min	Max	Unit	Note
tRC	Row cycle time	60		ns	
tRFC	Refresh row cycle time	72		ns	
tRAS	Row active time	42	70K	ns	
tRCD	/RAS to /CAS delay	18		ns	
tRP	Row precharge time	18		ns	
tRRD	Row active to Row active delay	15		ns	
tWR	Write recovery time	15		ns	
tWTR	Internal write to read command delay	1		tCK	
tCK	Clock cycle time	CL=2.0	7.5	13	ns
	Clock cycle time	CL=2.5	6	13	ns
tCH	Clock high level width	0.45	0.55	tCK	4
tCL	Clock low level width	0.45	0.45	0.55	4
tDQSCK	DQS-out access time from CK, /CK	-0.6	+0.6	ns	
tAC	Output data access time from CK, /CK	-0.7	+0.7	ns	
tDQSQ	Data strobe edge to output data edge		+0.45	ns	
tRPRE	Read Preamble	0.9	1.1	tCK	
tRPST	Read Postamble	0.4	0.6	tCK	
tDQSS	CK to valid DQS-in	0.75	1.25	tCK	
tWPRES	DQS-in setup time	0		ns	2
tWPRE	Write Preamble	0.25		tCK	
tDSS	DQS falling edge to CK rising-setup time	0.2		tCK	
tDSH	DQS falling edge from CK rising-hold time	0.2		tCK	
tDQSH	DQS-in high level width	0.35		tCK	
tDQSL	DQS-in low level width	0.35		tCK	
tIS(fast)	Address and Control Input setup time	0.75		ns	5
tIH(fast)	Address and Control Input hold time	0.75		ns	5
tIS(slow)	Address and Control Input setup time	0.8		ns	5
tIH(slow)	Address and Control Input hold time	0.8		ns	5
tHZ	Data-out high impedance time from CK,/CK	-0.7	0.7	ns	
tLZ	Data-out low impedance time from CK,/CK	-0.7	0.7	ns	
tMRD	Mode register set cycle time	2		tCK	
tDS	DQ and DM setup time to DQS	0.45		ns	6,7,8
tDH	DQ and DM hold time to DQS	0.45		ns	6,7,8
tDIPW	DQ and DM input pulse width	1.75		ns	
tIPW	Control and Address input pulse width for each input	2.2		ns	
tXSNR	Exit self refresh to non-read command	75		ns	
tXSRD	Exit self refresh to read command	200		Cycle	
tREFI	Refresh interval time		7.8	µs	1
tQH	Output DQS valid window	tHPmin -tQHS		ns	
tHP	Clock half period	tCLmin or tCHmin		ns	
tQHS	Data hold skew factor		0.55	ns	
tWPST	DQS write postamble time	0.4	0.6	tCK	3
tRAP	Active to autoprecharge delay	18		ns	
N/A	Data valid output window		tQH - tDQSQ	ns	9

Notes:

1. The refresh period is 64ms. This equates to an average refresh rate of 7.8125 μ s. However, an AUTO REFRESH command must be asserted at least once every 70.3 μ s; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. For registered DIMMs, tCL and tCH are \geq 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.

5. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate (V/ns)	delta tIS (ps)	delta tIH (ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t IS /t IH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

6. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate (V/ns)	delta tDS (ps)	delta tDH (ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t DS /t DH in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Plateau Derating

I/O Input Level (mV)	delta tDS (ps)	delta tDH (ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF \pm 310mV for a duration of up to 2ns.

8. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate (ns/V)	delta tDS (ps)	delta tDH (ps)
0	0	0
± 0.25	+50	+50
± 0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

9. The valid data window is derived by achieving other specifications: tHP (tCK/2), tDQSQ, and tQH (tQH = tHP - tQHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain.

REVISION HISTORY

Rev. Change Description from Previous Revision

- 101 03/04/2003. Initial release.
- 102 09/27/2005. Updated to current die revs. U option added.
- 103 10/04/2005. Block diagram corrected from two ranks to one rank.
- 104 11/30/2005. Updated to latest format and die revisions. W option added.
- 105 07/30/2007. Logo updated. Byte 72 of SPD updated to include Malaysia.

DISCLAIMER OF LIABILITY

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