64M X 72 Bits (512MB) DDR SDRAM 184-Pin 1U Registered DIMM ECC (PC2700)

FEATURES

- PC2700 Compliant
  (DDR333B 167MHz-6ns@CL= 2.5)
- 184-Pin DIMM form factor
- Industrial operating temperature option:
  (W) = -40°C to +95°C (Ambient)
- Auto and self refresh capability
  (8192 cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- +2.5V ± 0.2V V_{DD} and V_{DDQ}
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM
- ECC
- RoHS Compliant, Lead Free

GENERAL DESCRIPTION

The SL72E8M64M8M-B06EW(W)U is a 64M x 72 bits Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Dual In-line Memory Module (DIMM).

This module consists of nine CMOS 16M x 8 bits x 4 banks DDR SDRAMs in lead-free 66-pin 400-mil TSOP-II packages. The DDR SDRAMs are mounted on a 184-pin glass epoxy substrate. The user has the option of choosing industrial temperature rated SDRAM components.

A serial EEPROM using the two pin IIC protocol is also mounted to provide for the Serial Presence Detects (SPD). PLL circuits supply clocks to the DDR SDRAMs. Decoupling capacitors of 0.22µF are also mounted. Damping resistors are added to the DQ, DM, and DQS signals.

All control and address signals are re-driven through a register to the SDRAM devices. The control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock).

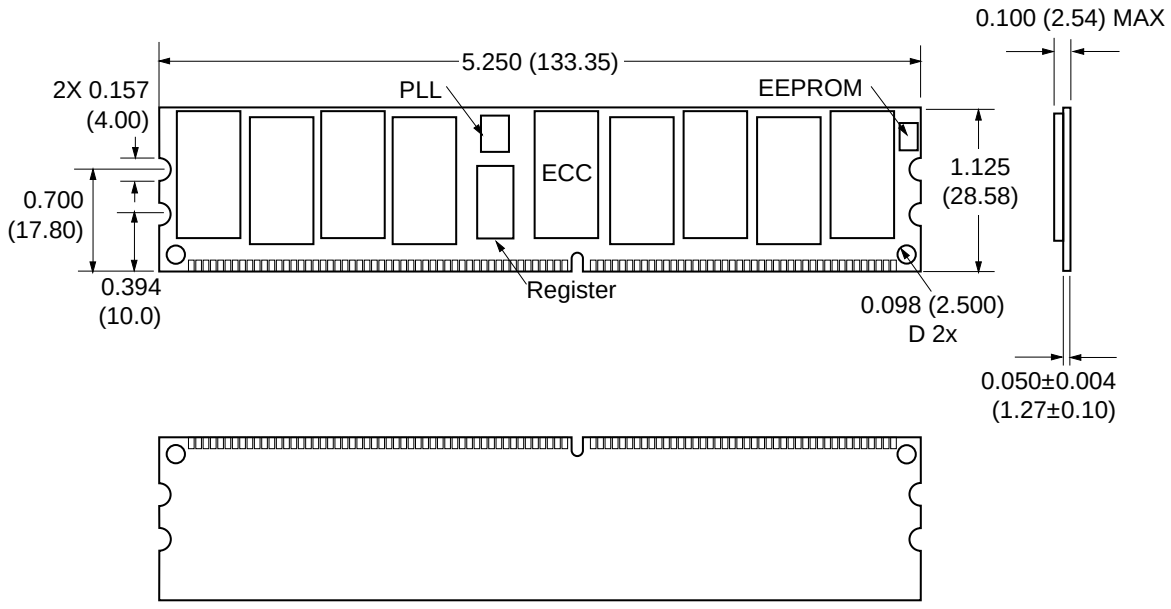
The module has gold edge connections and is intended for mounting into 184-pin DIMM edge connector sockets keyed for 2.5V V_{DD} and V_{DDQ}.

ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72E8M64M8M-B06EW(W)U	2.5	167	2.7 GB/s

PACKAGE DIMENSIONS

Units are in inches (millimeters). Tolerances are ±0.005 (±0.127) unless otherwise specified.



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PIN CONFIGURATION (*=Not Used; /=Active Low)

Pinout

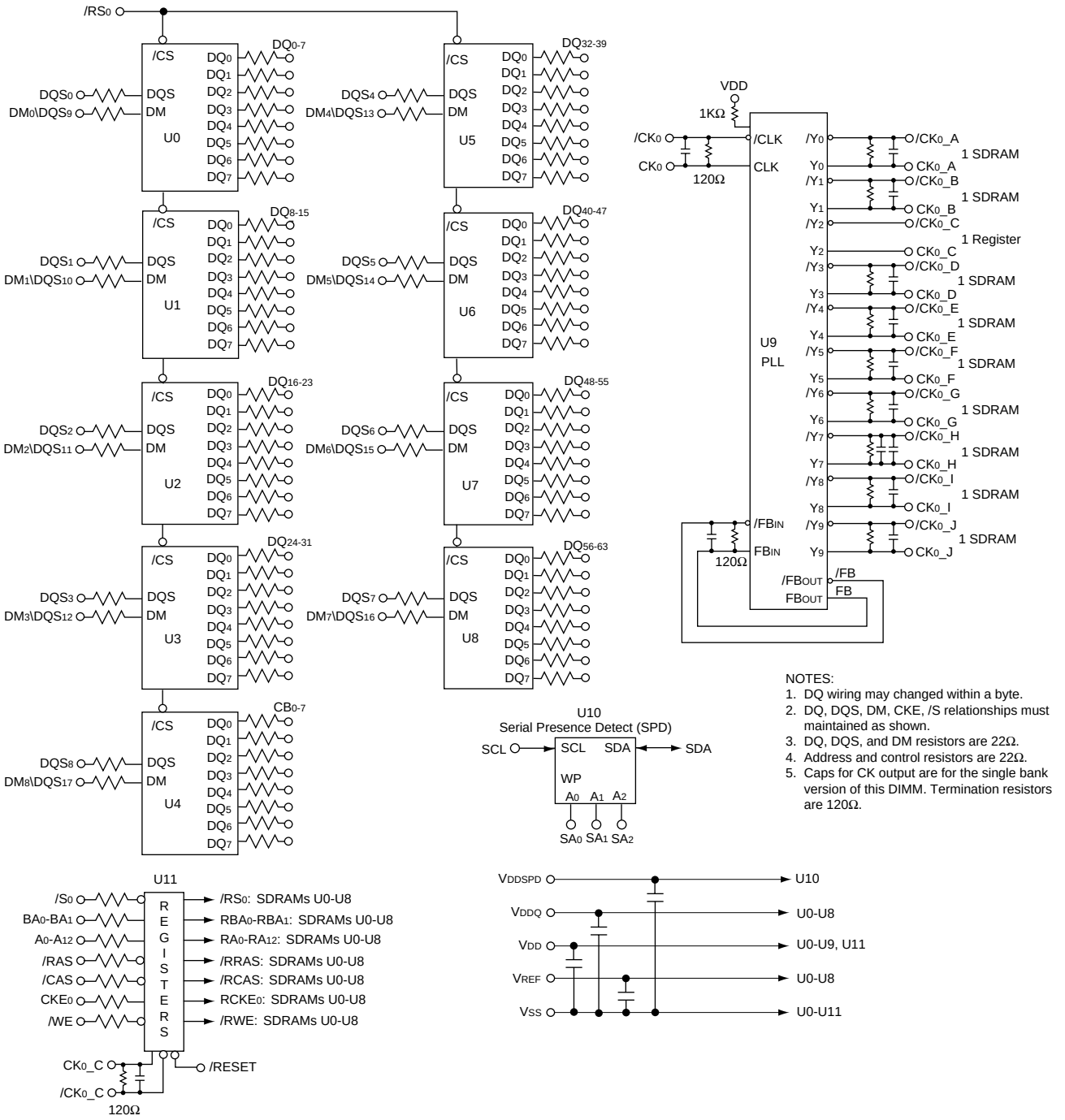
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	93	V_{SS}	32	A_5	124	V_{SS}	62	V_{DDQ}	154	/RAS
2	DQ_0	94	DQ_4	33	DQ_{24}	125	A_6	63	/WE	155	DQ_{45}
3	V_{SS}	95	DQ_5	34	V_{SS}	126	DQ_{28}	64	DQ_{41}	156	V_{DDQ}
4	DQ_1	96	V_{DDQ}	35	DQ_{25}	127	DQ_{29}	65	/CAS	157	$/S_0$
5	DQS_0	97	DM_0\DQS_9	36	DQS_3	128	V_{DDQ}	66	V_{SS}	158	$/S_1$*
6	DQ_2	98	DQ_6	37	A_4	129	DM_3\DQS_{12}	67	DQS_5	159	DM_5\DQS_{14}
7	V_{DD}	99	DQ_7	38	V_{DD}	130	A_3	68	DQ_{42}	160	V_{SS}
8	DQ_3	100	V_{SS}	39	DQ_{26}	131	DQ_{30}	69	DQ_{43}	161	DQ_{46}
9	NC	101	NC	40	DQ_{27}	132	V_{SS}	70	V_{DD}	162	DQ_{47}
10	/RESET	102	NC	41	A_2	133	DQ_{31}	71	$/S_2$*	163	$/S_3$*
11	V_{SS}	103	A_{13}*	42	V_{SS}	134	CB_4	72	DQ_{48}	164	V_{DDQ}
12	DQ_8	104	V_{DDQ}	43	A_1	135	CB_5	73	DQ_{49}	165	DQ_{52}
13	DQ_9	105	DQ_{12}	44	CB_0	136	V_{DDQ}	74	V_{SS}	166	DQS_3
14	DQS_1	106	DQ_{13}	45	CB_1	137	CK_0	75	CK_2*	167	FETEN*
15	V_{DDQ}	107	DM_1\DQS_{10}	46	V_{DD}	138	$/CK_0$	76	$/CK_2$*	168	V_{DD}
16	CK_1*	108	V_{DD}	47	DQS_8	139	V_{SS}	77	V_{DDQ}	169	DM_6\DQS_{15}
17	$/CK_1$*	109	DQ_{14}	48	A_0	140	DM_8\DQS_{17}	78	DQS_6	170	DQ_{54}
18	V_{SS}	110	DQ_{15}	49	CB_2	141	A_{10}	79	DQ_{50}	171	DQ_{55}
19	DQ_{10}	111	CKE_1*	50	V_{SS}	142	CB_6	80	DQ_{51}	172	V_{DDQ}
20	DQ_{11}	112	V_{DDQ}	51	CB_3	143	V_{DDQ}	81	V_{SS}	173	NC
21	CKE_0	113	BA_2*	52	BA_1	144	CB_7	82	V_{DDID}*	174	DQ60
22	V_{DDQ}	114	DQ_{20}		**Key**		**Key**	83	DQ_{56}	175	DQ_{61}
23	DQ_{16}	115	A_{12}	53	DQ_{32}	145	V_{SS}	84	DQ_{57}	176	V_{SS}
24	DQ_{17}	116	V_{SS}	54	V_{DDQ}	146	DQ_{36}	85	V_{DD}	177	DM_7\DQS_{16}
25	DQS_2	117	DQ_{21}	55	DQ_{33}	147	DQ_{37}	86	DQS_7	178	DQ_{62}
26	V_{SS}	118	A_{11}	56	DQS_4	148	V_{DD}	87	DQ_{58}	179	DQ_{63}
27	A_9	119	DM_2\DQS_{11}	57	DQ_{34}	149	DM_4\DQS_{13}	88	DQ_{59}	180	V_{DDQ}
28	DQ_{18}	120	V_{DD}	58	V_{SS}	150	DQ_{38}	89	V_{SS}	181	SA_0
29	A_7	121	DQ_{22}	59	BA_0	151	DQ_{39}	90	NC	182	SA_1
30	V_{DDQ}	122	A_8	60	DQ_{35}	152	V_{SS}	91	SDA	183	SA_2
31	DQ_{19}	123	DQ_{23}	61	DQ_{40}	153	DQ_{44}	92	SCL	184	V_{DDSPD}

Pin Description

Pin Symbol	Pin Description
A_0-A_{11}, A_{12}, A_{13}*	SDRAM address bus
BA_0-BA_1, BA_2*	SDRAM bank select
DQ_0-DQ_{63}	DIMM memory data bus
CB_0-CB_7	DIMM ECC check bits
/RAS	SDRAM row address strobe
/CAS	SDRAM column address strobe
/WE	SDRAM write strobe
$/S_0$, $/S_1$*, $/S_2$*, $/S_3$*	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)
CKE_0, CKE_1*	SDRAM clock enable lines
DQS_0-DQS_8	SDRAM low data strobes
$DM_{(0-8)}$\$DQS_{(9-17)}$	SDRAM low data masks\high data strobes (x4, x8-based x72 DIMMs)
V_{DDID}*	V_{DD} Identification flag
CK_0, CK_1*, CK_2*	SDRAM clock (positive line of differential pair)

Pin Symbol	Pin Description
$/CK_0$, $/CK_1$*, $/CK_2$*	SDRAM clock (negative line of differential pair)
SCL	IIC serial bus clock for EEPROM
SDA	IIC serial bus data line for EEPROM
SA_0-SA_2	IIC slave address select for EEPROM
V_{DD}	SDRAM positive power supply
V_{DDQ}	SDRAM I/O driver positive power supply
V_{REF}	SDRAM I/O reference supply
V_{SS}	Power supply return (ground)
V_{DDSPD}	Serial EEPROM positive power supply ($2.2V \le V_{DDSPD} \le 5.5V$)
NC	Spare pins (no connect)
/RESET	Reset pin (forces register inputs low)
FETEN*	FET enable line

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. DQ wiring may changed within a byte.
2. DQ, DQS, DM, CKE, /S relationships must maintained as shown.
3. DQ, DQS, and DM resistors are 22Ω.
4. Address and control resistors are 22Ω.
5. Caps for CK output are for the single bank version of this DIMM. Termination resistors are 120Ω.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: IIC; Current sink capability of SDA driver ≤3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
		DDR333B	DDR333B
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	DDR SDRAM	07h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	11	0Bh
5	# of physical banks on this assembly	1 bank	01h
6	Data width of this assembly	72 bits	48h
7	…Data width of this assembly (continued)	—	00h
8	Voltage interface level of this assembly	SSTL 2.5V	04h
9	SDRAM cycle time at CL=2.5 (t_{CYC})	6ns	60h
10	SDRAM access time from clock at CL=2.5 (t_{AC})	0.7ns	70h
11	DIMM configuration type	ECC	02h
12	Refresh rate/type	7.8µs, Self -refresh	82h
13	SDRAM width	8 bits	08h
14	Error Checking SDRAM data width	8 bits	08h
15	Min. CLK delay for back-to-back rand. col. addr.	t_{CCD}=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	2,4,8	0Eh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5	0Ch
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 1	02h
21	SDRAM module attributes	Registered with Differential clock, PLL	26h
22	SDRAM device attributes: general	V_{DD}±0.2V	00h
23	Minimum clock cycle time at CL=2 (t_{CYC})	7.5ns	75h
24	Max. data access time form clock at CL=2 (t_{AC})	0.7ns	70h
25	Minimum clock cycle time at CL=1.5 (t_{CYC})	N/A	00h
26	Max. data access time from clock at CL=1.5 (t_{AC})	N/A	00h
27	Minimum row precharge time (t_{RP})	18ns	48h
28	Minimum row active to row active delay (t_{RRD})	12ns	30h
29	Minumum RAS to CAS (t_{RCD})	18ns	48h
30	Minumum RAS pulse width (t_{RAS})	42ns	2Ah
31	Module bank density	512MB	80h
32	Min. command and address signal setup time (t_{IS})	0.75ns	75h
33	Min. command and address signal hold time (t_{IH})	0.75ns	75h
34	Min. data/data mask signal input setup time (t_{DS})	0.45ns	45h
35	Min. data/data mask signal input hold time (t_{DH})	0.45ns	45h

continued on the next page

SERIAL PRESENCE DETECT INFORMATION (continued)

Byte #	Function Described	Function Supported	Hex Value
		DDR333B	DDR333B
41	Row cycle time (t_{RC})	65ns	41h
42	Auto refresh cycle time (t_{RFC})	75ns	4Bh
43	Maximum SDRAM device cycle time (t_{CK_MAX})	12ns	30h
44	DQS-DQ skew (t_{DQSQ})	0.50ns	32h
45	SDRAM device data hold skew factor (t_{QHS})	0.75ns	75h
46-61	Reserved		00h
62	SPD revision	JEDEC 1	00h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71			00h
72	Manufacturing location	STEC USA	01h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)	xxh
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	w w
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-127	Manufacturer's specific data		xxh
128-255	Open for Customer Use	Undefined	FFh

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional Operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time may affect device reliability.

Symbol	Parameter	Min	Max	Units
VIN, VOUT	VDD Supply Voltage Relative to VSS	-0.5	3.6	V
VDD	VDDQ Supply Voltage Relative to VSS	-1.0	3.6	V
VDDQ	VDDL Supply Voltage Relative to VSS	-1.0	3.6	V
PD	Power Dissapation	13.5		W
IOS	Short Circuit Current	50		mA
TSTG	Storage Temperature	-55	100	°C
TOPR	SDRAM Device Operating Temperature			
	Commercial Operating Temperature	0	85	°C
	Industrial Operation Temperature	0	95	°C
Ta	Ambient Operating Temperature			
	Commercial Operating Temperature	0	55	°C
	Industrial Operation Temperature	-40	85	°C

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

Recommended operating conditions (Voltage referenced to V_{SS}=0V. T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (for device with a nominal V_{DD} of 2.5V	V_{DD}	2.3	2.7	V	
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	$V_{DD}Q$/2-50mV	$V_{DD}Q$/2+50mV	V	1
I/O Termination voltage (system)	V_{TT}	V_{REF}–0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	$V_{DD}Q$+0.3	V	
Input logic low voltage	V_{IL}(DC)	–0.3	V_{REF}–0.15	V	
Input voltage level, CK and /CK	V_{IN}(DC)	–0.3	$V_{DD}Q$+0.3	V	
Input differential voltage, CK and /CK	V_{ID}(DC)	0.3	$V_{DD}Q$+0.6	V	3
Input leakage current	I_L	-5	5	µA	
Output leakage current	I_{OZ}	-5	5	µA	
Output high current (V_{OUT}=V_{TT}+0.84V)	I_{OH}	-16.8		mA	
Output low current (V_{OUT}=V_{TT}–0.84V)	I_{OL}	16.8		mA	

1. V_{REF} is expected to be equal to 0.5*V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted. VDD=2.7, T=10°C; Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.)

Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; t RC = t RC (MIN); t CK = t CK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles;	IDD0	1165	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; t RC = t RC (MIN); t CK = t CK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle	IDD1	1390	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t CK = t CK (MIN); CKE = (LOW)	IDD2P	45	mA
IDLE STANDBY CURRENT: CS# = HIGH; All banks idle; t CK = t CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	310	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t CK = t CK (MIN); CKE = LOW	IDD3P	270	mA
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank; Active-Precharge; t RC = t RAS (MAX); t CK = t CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	490	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); IOUT = 0mA	IDD4R	1525	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	1750	mA
AUTO REFRESH CURRENT t RC = t RC(MIN)	IDD5	2290	mA
SELF REFRESH CURRENT: CKE<=0.2V	IDD6	45	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, t RC = t RC (MIN); t CK = t CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7A	3640	mA

Detailed Test Conditions: DDR SDRAM IDD1

(A=Activate, R=Read, W=Write, P=Precharge, N=NOP)

1. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout=0mA.
2. Timing patterns:
   - DDR333B (167MHz, CL=2.5): tCK=6ns, CL=2.5, BL=4, tRCD=10*tCK, tRAS=7*tCK,
     Read: A0 N N R0 N P0 N N N A0 N —repeat the same timing with random address changing,
     50% of data changing at every burst.

Detailed Test Conditions: DDR SDRAM IDD7A

(A=Activate, R=Read, W=Write, P=Precharge, N=NOP)

1. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout=0mA.
2. Timing patterns:
   - DDR333B (167MHz, CL=2.5): tCK=6ns, CL=2.5, BL=4, tRRD=2*tCK, tRCD=3*tCK, Read with Autoprecharge,
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 — repeat the same timing with random address changing,
     100% of data changing at every burst.

AC OPERATING CONDITIONS

(V_{DD}=V_{DD}Q=2.5V, T_A=25°C, f=1MHz)

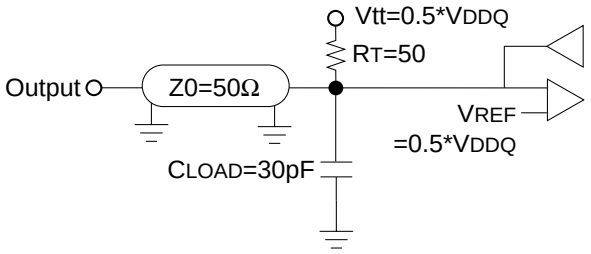
Parameter/Condition	Symbol	Min	Max	Units	Note
Input High (Logic 1) Voltage, DQ, DQS, and DM signals	VIH(AC)	VREF+0.31		V	1
Input Low (Logic 0) Voltage, DQ, DQS, and DM signals	VIL(AC)		VREF-0.31	V	2
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ+0.6	V	3
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	4

1. Vih(max)=4.2V. The overshoot voltage duration is <=3ns at VDD.
2. Vil(min=–1.5V. The undershoot voltage duration is <=3ns at VSS.
3. VID is the magnitude of the difference between the input level on CK and the input on /CK.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS

(V_{DD}=V_{DD}Q=2.5V, T_A=0°C to 70°C)

Parameter	Value	Unit
Input reference voltage for Clock	0.5*V_{DDQ}	V
Input signal maximum peak swing	1.5	V
Input signal minimum slew rate	0.5	V/ns
Input levels (V_{IH}/V_{IL})	V_{REF}+0.31/V_{REF}–0.31	V
Input timing measurement ref. level	V_{REF}	V
Output timing measurement ref. level	V_{TT}	V
Output load condition	See Load Circuit	



Output Load Circuit (SSTL_2)

INPUT/OUTPUT CAPACITANCE

(V_{DD}=V_{DD}Q=2.5V, T_A=25°C, f=1MHz)

Parameter	Symbol	Max	Units
Input Capacitance (A_0-A_{12}, BA_0, BA_1, /RAS, /CAS, /WE)	C_{IN1}	15	pF
Input Capacitance (CKE_0)	C_{IN2}	15	pF
Input Capacitance (/S_0, /S_1)	C_{IN3}	15	pF
Input Capacitance (CK_0)	C_{IN4}	20	pF
Input Capacitance (DM_0\$DQS_9$-$DM_8$\$DQS_{17}$, DQS_0-DQS_8)	C_{IN5}	10	pF
Data Input/Output Capacitance (DQ_0-DQ_{63})	C_{OUT1}	10	pF
Data Input/Output Capacitance (CB_0-CB_7)	C_{OUT2}	10	pF

AC TIMING PARAMETERS (These AC characteristics were tested on the Component)

Parameter	Symbol	Min	Max	Units
Access window of DQs from CK/CK#	t AC	-0.7	+0.7	ns
CK high-level width	t CH	0.45	0.55	t CK
CK low-level width	t CL	0.45	0.55	t CK
Clock cycle time CL = 2.5	t CK (2.5)	6	12	ns
CL = 2	t CK (2)	7.5	12	ns
DQ and DM input hold time relative to DQS	t DH	0.45		ns
DQ and DM input setup time relative to DQS	t DS	0.45		ns
DQ and DM input pulse width (for each input)	t DIPW	1.75		ns
Access window of DQS from CK/CK#	t DQSCK	-0.60	+0.60	ns
DQS input high pulse width	t DQSH	0.35		t CK
DQS input low pulse width	t DQSL	0.35		t CK
DQS-DQ skew, DQS to last DQ valid, per group, per access	t DQSQ		0.45	ns
Write command to first DQS latching transition	t DQSS	0.75	1.25	CK
DQS falling edge to CK rising - setup time	t DSS	0.2		t CK
DQS falling edge from CK rising - hold time	t DSH	0.2		t CK
Half clock period	t HP	t CH,t CL		ns
Data-out high-impedance window from CK/CK#	t HZ	-0.70	+0.70	ns
Data-out low-impedance window from CK/CK#	t LZ	-0.70	+0.70	ns
Address and control input hold time (fast slew rate)	t IH F	0.75		ns
Address and control input setup time (fast slew rate)	t IS F	0.75		ns
Address and control input hold time (slow slew rate)	t IH S	0.80		ns
Address and control input setup time (slow slew rate)	t IS S	0.80		ns
Address and control input pulse width	t IPW	2.2		ns
LOAD MODE REGISTER command cycle time	t MRD	12		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t QH	t HP - t QHS		ns
Data Hold Skew Factor	t QHS		0.55	ns
ACTIVE to AUTOPRECHARGE command	t RAP	18		ns
ACTIVE to PRECHARGE command	t RAS	42	70,000	ns
ACTIVE to ACTIVE/AUTO REFRESH command period	t RC	60		ns
AUTO REFRESH command period	t RFC	72		ns
ACTIVE to READ or WRITE delay	t RCD	18		ns
PRECHARGE command period	t RP	18		ns
DQS read preamble	t RPRE	0.9	1.1	t CK
DQS read postamble	t RPST	0.4	0.6	t CK
ACTIVE bank *a* to ACTIVE bank *b* command	t RRD	12		ns
DQS write preamble	t WPRE	0.25		t CK
DQS write preamble setup time	t WPRES	0		ns
DQS write postamble	t WPST	0.4	0.6	t CK
Write recovery time	t WR	15		ns
Internal WRITE to READ command delay	t WTR	1		t CK
Data valid output window	na	t QH - t DQSQ		ns
REFRESH to REFRESH command interval	t REFC	70.3		µs
Average periodic refresh interval	t REFI	7.8		µs
Terminating voltage delay to VDD	t VTD	0		ns
Exit SELF REFRESH to non-READ command	t XSNR	75		ns
Exit SELF REFRESH to READ command	t XSRD	200		t CK

REVISION HISTORY

Rev.	Change Description from Previous Revision
-101	07/15/2003. Initial Release.
-102	10/10/2003. P/N corrected to -B06EW. VDDSPD range added to Pin Discription table. Capacitance recalculated according to pF values for PCB: 15pF for clock, and 5pF for data.
-103	01/26/2007. Added second “W” designator to part number suffix and ordering information to indicate that the product can be ordered with industrial operating temperature grade components. Added the “U” designator to the part suffix to indicate the product is RoHS compliant, lead free.
-104	07/19/2007. Updated logo, web address and SPD.