

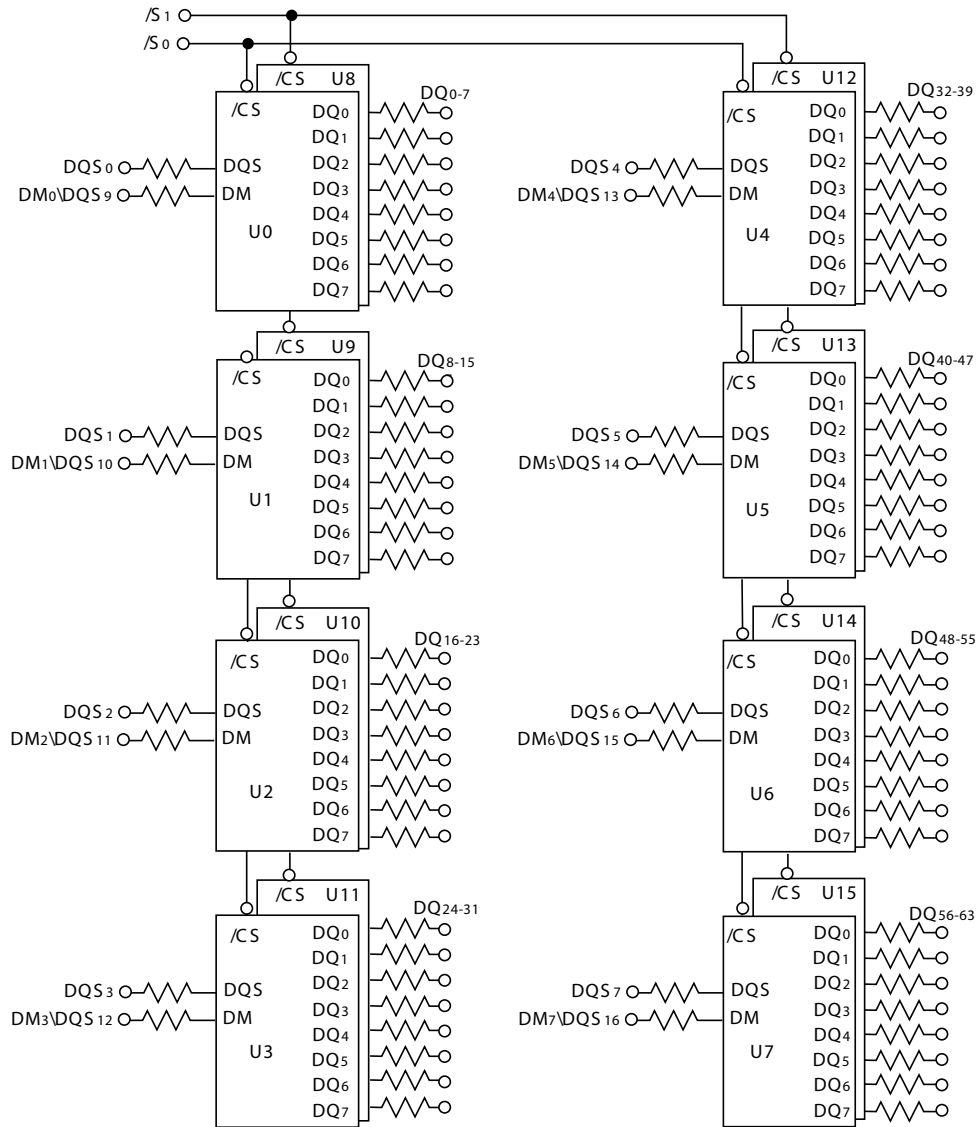
PIN CONFIGURATION (* = Not Used; / = Active Low; **Bold Lines = Key**)**PINOUT**

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	VSS	32	A5	124	VSS	62	VDDQ	154	/RAS
2	DQ0	94	DQ4	33	DQ24	125	A6	63	/WE	155	DQ45
3	VSS	95	DQ5	34	VSS	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	/CAS	157	/S0
5	DQS0	97	DM0\DQS9	36	DQS3	128	VDDQ	66	VSS	158	/S1
6	DQ2	98	DQ6	37	A4	129	DM3\DQS12	67	DQS5	159	DM5\DQS14
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	VSS
8	DQ3	100	VSS	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	VSS	70	VDD	162	DQ47
10	/RESET*	102	NC	41	A2	133	DQ31	71	/S2*	163	/S3*
11	VSS	103	A13*	42	VSS	134	CB4*	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	CB5*	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	CB0*	136	VDDQ	74	VSS	166	DQS3
14	DQS1	106	DQ13	45	CB1*	137	CK0	75	CK2	167	FETEN*
15	VDDQ	107	DM1\DQS10	46	VDD	138	/CK0	76	/CK2	168	VDD
16	CK1	108	VDD	47	DQS8*	139	VSS	77	VDDQ	169	DM6\DQS15
17	/CK1	109	DQ14	48	A0	140	DM8\DQS17*	78	DQS6	170	DQ54
18	VSS	110	DQ15	49	CB2*	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1	50	VSS	142	CB6*	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	CB3*	143	VDDQ	81	VSS	173	NC
21	CKE0	113	BA2*	52	BA1	144	CB7*	82	VDDID*	174	DQ60
22	VDDQ	114	DQ20	Key		Key		83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	VSS	84	DQ57	176	VSS
24	DQ17	116	VSS	54	VDDQ	146	DQ36	85	VDD	177	DM7\DQS16
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	VSS	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DM2\DQS11	57	DQ34	149	DM4\DQS13	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	VSS	150	DQ38	89	VSS	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	VDDQ	122	A8	60	DQ35	152	VSS	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

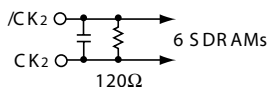
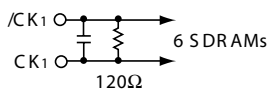
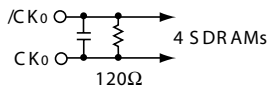
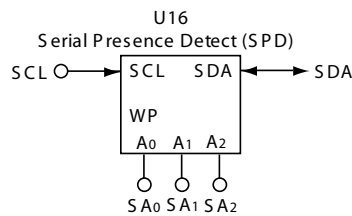
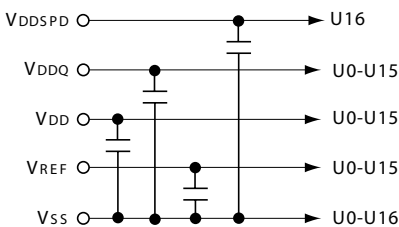
PIN DESCRIPTION

Pin Symbol	Pin Description	Pin Symbol	Pin Description
A0-A12, A13*	SDRAM Address Bus	/CK0, /CK1, /CK2	SDRAM Clock (Negative Line of Differential Pair)
BA0-BA1, BA2*	SDRAM Bank Select	SCL	IIC Serial Bus Clock for EEPROM
DQ0-DQ63	DIMM Memory Data Bus	SDA	IIC Serial Bus Data Line for EEPROM
CB0-CB7*	DIMM ECC Check Bits	SA0-SA2	IIC Slave Address Select for EEPROM
/RAS	SDRAM Row Address Strobe	VDD	SDRAM Positive Power Supply
/CAS	SDRAM Column Address Strobe	VDDQ	SDRAM I/O Driver Positive Power Supply
/WE	SDRAM Write Strobe	VREF	SDRAM I/O Reference Supply
/S0, /S1, /S2*, /S3*	SDRAM Chip Select Lines (Physical banks 0, 1, 2, and 3)	VSS	Power Supply Return (Ground)
CKE0, CKE1	SDRAM Clock Enable Lines	VDDSPD	Serial EEPROM Positive Power Supply (2.2V <= VDDSPD <= 5.5V)
DQS0-DQS7, DQS8*	SDRAM Low Data Strobes	NC	Spare Pins (no connect)
DM(0-7)\DQS(9-16), DM8\DQS17*	SDRAM Low Data Masks\High Data strobes (x4, x8-based x72 DIMMs)	/RESET*	Reset Pin (Forces Register Inputs Low)
VDDID*	VDD Identification Flag	FETEN*	FET Enable Line
CK0, CK1, CK2	SDRAM Clock (Positive Line of Differential Pair)		

FUNCTIONAL BLOCK DIAGRAM



- BA0-BA1 → BA0-BA1: SDRAMs U0-U15
- A0-A12 → A0-A12: SDRAMs U0-U15
- /RAS → /RAS: SDRAMs U0-U15
- /CAS → /CAS: SDRAMs U0-U15
- CKE0 → CKE0: SDRAMs U0-U7
- CKE1 → CKE1: SDRAMs U8-U15
- /WE → /WE: SDRAMs U0-U15



- NOTES:
1. DQ wiring may be changed within a byte.
 2. DQ, DQS, DM, CKE, /S relationships must be maintained as shown.
 3. DQ, DQS, and DM resistors are 22Ω.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: IIC; Current sink capability of SDA driver $\leq 3\text{mA}$; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	No. of Bytes Written into Serial Memory at Module Manufacturer	128	80h
1	Total No. of Bytes of SPD Memory Device	256 (2K-Bit)	08h
2	Fundamental Memory Type	DDR SDRAM	07h
3	No. of Row Addresses on Assembly	13	0Dh
4	No. of Column Addresses on Assembly	11	0Bh
5	No. of Physical Banks on Assembly	2	02h
6	Data Width of Assembly	x64	40h
7	Data Width of Assembly (Continued)	-	00h
8	Voltage Interface Level of Assembly	SSTL 2.5V	04h
9	SDRAM Cycle Time at CL = 3 (tCYC)	5.0ns	50h
10	SDRAM Access Time from clock at CL = 3 (tAC)	0.7ns	70h
11	DIMM Configuration Type	None	00h
12	Refresh Rate/Type	7.8 μs , SELF	82h
13	SDRAM Width	8 bits	08h
14	Error Checking SDRAM Data Width	None	00h
15	Min. CLK Delay for Back-to-Back Rand. Col. Addr.	tCCD = 1 CLK	01h
16	SDRAM Device Attributes: Burst Lengths Supported	2, 4, 8	0Eh
17	SDRAM Device Attributes: No. of Banks on SDRAM Device	4	04h
18	SDRAM Device Attributes: CAS Latency	CAS Latency = 3	18h
19	SDRAM Device Attributes: CS Latency	CS Latency = 0	01h
20	SDRAM Device Attributes: Write Latency	Write Latency = 1	02h
21	SDRAM Module Attributes	Differential Clock	20h
22	SDRAM Device Attributes: General	VDD +/- 0.1V	00h
23	Minimum Clock Cycle Time at CL = 2.5 (tCYC)	6.0ns	60h
24	Maximum Data Access Time from Clock at CL = 2.5 (tAC)	0.70ns	70h
25	Minimum Clock Cycle Time at CL = 1.5 (tCYC)	N/A	00h
26	Maximum Data Access Time from Clock at CL = 1.5 (tAC)	N/A	00h
27	Minimum Row Precharge Time (tRP)	20ns	3Ch
28	Minimum Row Active to Row Active Delay (tRRD)	10ns	28h
29	Minimum RAS to CAS (tRCD)	20ns	3Ch
30	Minimum RAS Pulse Width (tRAS)	40ns	28h
31	Module Bank Density	512MB	80h
32	Minimum Command and Address Signal Setup Time (tAS)	0.6ns	60h
33	Minimum Command and Address Signal Hold Time (tAH)	0.6ns	60h
34	Minimum Data/Data Mask Signal Input Setup Time (tDS)	0.4ns	40h
35	Minimum Data/Data Mask Signal Input Hold Time (tDH)	0.4ns	40h

(Serial Presence Detect Information continued on next page.)

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte #	Function Described	Function Supported	Hex Value
36-40	Reserved for VCSDRAM	-	00h
41	Row Cycle Time (tRC)	60ns	3Ch
42	Auto Refresh Cycle Time (tRFC)	70ns	46h
43	Maximum SDRAM Device Cycle Time (tCK_MAX)	12ns	30h
44	DQS-DQ Skew (tDQSQ)	0.40ns	28h
45	SDRAM Device Data Hold Skew Factor (tQHS)	0.55ns	55h
46-61	Reserved	-	00h
62	SPD Revision	JEDEC 1	00h
63	Checksum for Bytes 0 - 62	JEDEC Calculation	xxh
64	Manufacturer's JEDEC ID Code per JEP-106E	Continuation Code	7Fh
65	Manufacturer's JEDEC ID Code (continued)	STEC's ID	A8h
66-71			00h
72	Manufacturing Location	STEC USA	01h
73-90	Manufacturer's Part Number		xxh
91	PCB Revision Code	Eng (00), Rev. A (01) Rev. B (02)	01h
92			
93	Manufacturing Date	Year (BCD)	yy
94		Calendar Week (BCD)	ww
95	Assembly Serial Number	Tester Number	ss
96		Serial Number (Bits 7-0)	ss
97		Serial Number (Bits 15-8)	ss
98		Serial Number (Bits 23-16)	ss
99-127	Manufacturer's Specific Data		xxh
128-255	Open for Customer's Use	Undefined	00h

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if *ABSOLUTE MAXIMUM RATINGS* are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods may affect device reliability.

Parameter	Symbol	Value	Unit
Voltage on any Pin Relative to VSS	VIN, VOUT	-0.5 to +3.6	V
Voltage on VDD Supply Relative to VSS	VDD	-1.0 to +3.6	V
Voltage on VDDQ Supply Relative to VSS	VDDQ	-1.0 to 3.6	V
Storage Temperature	TSTG	-55 to +150	°C
Power Dissipation	PD	24	W
Short Circuit Current	IOS	50	mA

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

Recommended operating conditions (Voltage referenced to VSS=0V. TA=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (For Device with a Nominal VDD of 2.5V)	VDD	2.5	2.7	V	
I/O Supply Voltage	VDDQ	2.5	2.7	V	
I/O Reference Voltage	VREF	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination Voltage (System)	VTT	VREF-0.04	VREF+0.04	V	2
Input Logic High Voltage	VIH(DC)	VREF+0.15	VDDQ+0.3	V	4
Input Logic Low Voltage	VIL(DC)	-0.3	VREF-0.15	V	4
Input Voltage Level, CK and /CK	VIN(DC)	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and /CK	VID(DC)	0.36	VDDQ+0.6	V	3
Input Crossing Point Voltage, CK and /CK	VIX(DC)	1.15	1.35	V	5
Input Leakage Current	IL	-32	32	µA	
Output Leakage Current	IOZ	-10	10	µA	
Output High Current (VOUT=VTT+0.84V) (Normal Strength Driver)	IOH	-16.8		mA	
Output Low Current (VOUT=VTT-0.84V) (Normal Strength Driver)	IOL	16.8		mA	
Output High Current (VOUT=VTT+0.45V) (Half Strength Driver)	IOH	-9		mA	
Output Low Current (VOUT=VTT-0.45V) (Normal Strength Driver)	IOL	9		mA	

Notes:

- Includes $\pm 25\text{mV}$ margin for DC offset on VREF, and a combined total of $\pm 50\text{mV}$ margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of $\leq 3\text{nH}$.
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
- VID is the magnitude of the difference between the input level on CK and the input level on /CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHz.
- The value of VIX is expected to equal $0.5 \cdot \text{VDDQ}$ of the transmitting device and must track variations in the dc level of the same.
- These characteristics obey the SSTL-2 class II standards.

DC CHARACTERISTICS

Recommended operating conditions unless otherwise noted; Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; t RC = t RC (MIN); t CK = t CK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;	IDD0	2080	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; t RC = t RC (MIN); t CK = t CK (MIN); IOU = 0mA; Address and control inputs changing once per clock cycle	IDD1	2240	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t CK = t CK (MIN); CKE = (LOW)	IDD2P	80	mA
IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	480	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t CK = t CK (MIN); CKE = LOW	IDD3P	560	mA
ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; t RC = t RAS (MAX); t CK = t CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	1520	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); IOU = 0mA	IDD4R	2360	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	2680	mA
AUTO REFRESH CURRENT: t RC = t RC(MIN)	IDD5	2880	mA
SELF REFRESH CURRENT: CKE <= 0.2V	IDD6	80	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, t RC = t RC (MIN); t CK = t CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7A	4200	mA

AC OPERATING CONDITIONS

(VDD=VDDQ=2.5V, TA=25°C, f=1MHz)

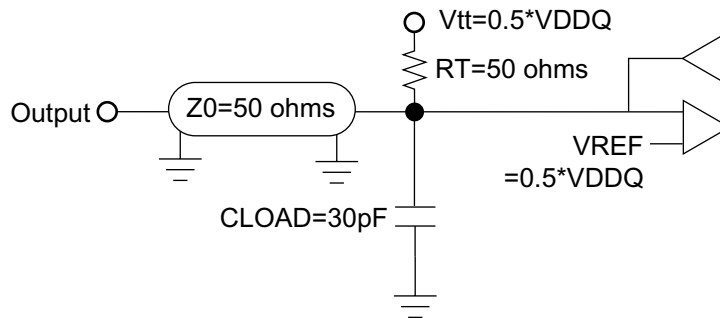
Parameter/Condition	Symbol	Min	Max	Units	Note
Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	VIH(AC)	VREF+0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals	VIL(AC)		VREF-0.31	V	3
Input Differential Voltage, CK and /CK Inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and /CK Inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Notes:

- VID is the magnitude of the difference between the input level on CK and the input on /CK.
- The value of V IX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS(V_{DD}=V_{DDQ}=2.5V, T_A=0°C to 70°C)

Parameter	Value	Unit
Input Reference Voltage for Clock	0.5*V _{DDQ}	V
Input Signal Maximum Peak Swing	1.5	V
Input Signal Minimum Slew Rate	0.5	V/ns
Input Levels (V _{IH} /V _{IL})	V _{REF} +0.31/V _{REF} -0.31	V
Input Timing Measurement Ref. Level	V _{REF}	V
Output Timing Measurement Ref. Level	V _{TT}	V
Output Load Condition	See Load Circuit	



Output Load Circuit (SSTL_2)

INPUT/OUTPUT CAPACITANCE(V_{DD}=V_{DDQ}=2.5V, T_A=25°C, f=1MHz)

Parameter	Symbol	Max	Units
Input Capacitance (A0-A12, BA0, BA1, /RAS, /CAS, /WE)	CIN1	78	pF
Input Capacitance (CKE0, CKE1)	CIN2	54	pF
Input Capacitance (/S0, /S1)	CIN3	54	pF
Input Capacitance (CK0-CK3, /CK0-/CK3)	CIN4	33	pF
Data and DQS I/O Capacitance (DQ0-DQ63, DQS0-DQS17)	COUT	15	pF
Input Capacitance (DM0-DM8)	CIN5	15	pF

AC TIMING PARAMETERS (These AC characteristics were tested on the component.)

Symbol	Parameter	Min	Max	Unit	Note
tRC	Row Cycle Time	60		ns	
tRFC	Refresh Row Cycle Time	70		ns	
tRAS	Row Active Time	40	120K	ns	
tRCD	/RAS to /CAS Delay	20		ns	
tRP	Row Precharge Time	20		ns	
tRRD	Row Active to Row Active Delay	10		ns	
tWR	Write Recovery Time	15		ns	
tWTR	Internal Write to Read Command Delay	2		tCK	
tCCD	Col. Address to Col. Address Delay	1		tCK	
tCK	Clock Cycle Time				
	CL = 3.0	5	12	ns	5
tCK	Clock Cycle Time				
	CL = 2.5	6	12	ns	5
tCH	Clock High Level Width	0.45	0.55	tCK	
tCL	Clock Low Level Width	0.45	0.55	tCK	
tDQSCK	DQS-Out Access Time from CK, /CK	-0.55	+0.55	ns	
tAC	Output Data Access Time from CK, /CK	-0.70	+0.70	ns	
tDQSQ	Data Strobe Edge to Output Data Edge		0.4	ns	5
tRPRE	Read Preamble	0.9	1.1	tCK	
tRPST	Read Postamble	0.4	0.6	tCK	
tDQSS	CK to Valid DQS-In	WL-0.25	WL+0.25	tCK	
tWPRES	DQS-In Setup Time	0		ns	2
tWPRE	Write Preamble	0.25		tCK	
tDSS	DQS Falling Edge to CK Rising-Setup Time	0.2		tCK	
tDSH	DQS Falling Edge from CK Rising-Hold Time	0.2		tCK	
tDQSH	DQS-In High Level Width	0.35		tCK	
tDQSL	DQS-In Low Level Width	0.35		tCK	
tDSC	DQS-In Cycle Time	0.9	1.1	tCK	
tIS	Address and Control Input Setup Time	0.6		ns	6
tIH	Address and Control Input Hold Time	0.6		ns	6
tHZ	Data-Out High Impedance Time from CK, /CK		tAC max	ps	
tLZ	Data-Out Low Impedance Time from CK, /CK	tAC min	tAC max	ps	
tMRD	Mode Register Set Cycle Time	2		tCK	
tDS	DQ and DM Setup Time to DQS	0.4		ns	7, 8, 9
tDH	DQ and DM Hold Time to DQS	0.4		ns	7, 8, 9
tDIPW	DQ and DM Input Pulse Width	0.35		tCK	
tIPW	Control and Address Input Pulse Width for Each Input	0.6		tCK	
tXPNR	Exit Precharge Power Down to any Command	2		tCK	
tXSC	Exit Self Refresh to any Command	200		tCK	
tREF	Refresh Interval Time	7.8		μs	1
tQH	Output DQS Valid Window	tHPmin -tQHS		ns	
tHP	Clock Half Period	tCLmin or tCHmin		ns	
tQHS	Data Hold Skew Factor		0.55	ns	
tWPST	DQS Write Postamble Time	0.4	0.6	tCK	3
tRAP	Active to Autoprecharge Delay	tRCD min		ns	
tDAL	Autoprecharge Write Recovery + Precharge Time	(tWR/tCK) +(tRP/tCK)		tCK	

Notes:

1. Maximum burst refresh of 8k.
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with tRCD satisfied after this command.
5. For registered DIMMs, tCL and tCH are $\approx 45\%$ of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	delta tIS	delta tIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase tIS /tIH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	delta tIS	delta tIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase tDS /tDH in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	delta tIS	delta tIH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ± 310 mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	delta tIS	delta tIH
(ns/V)	(ps)	(ps)
0	0	0
± 0.25	+50	+50
± 0.50	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as $1/\text{SlewRate1}-1/\text{SlewRate2}$. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = $-0/5\text{ns/V}$. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is for system simulation purpose. It is guaranteed by design.

REVISION HISTORY

Rev. Change Description from Previous Revision

- 101 09/05/03. Initial release.
- 102 10/14/03. SPD Bytes 10, 23, 24, 27, 29, and 43 corrected. Capacitance recalculated with new adders for PCB: 30pF address, 15pF clock, 5pF data.
- 103 02/20/04. SPD Bytes 16 and 18 corrected. VDDSPD specified in a range in Pin Description table. Component based specifications updated to latest die revision.
- 104 09/15/2006. Added "U" designator to part number to indicate RoHS compliance. Added standard RoHS statement to subtitle and description.
- 105 07/23/2007. Updated logo, web address and SPD.

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