

128M X 64 Bits (1GB) 144-Pin SDRAM SO-DIMM (PC133)

FEATURES

- PC133 Compliant ($t_{CYC}=7.5ns@CL=3$) (see *Ordering Information* for options)
- Burst Mode Operation
- Auto and self refresh capability (8192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V \pm 0.3V power supply
- MRS cycle with address key programs
 - Latency (access from column address)
 - Burst Length (1, 2, 4, 8, and Full Page)
 - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with 256 Byte EEPROM
- RoHS Compliant, lead-free

GENERAL DESCRIPTION

The SL64G7M128M8G-B75AVU is a 128M x 64 bit Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of eight IC Towers (stack of two SDRAMs) mounted on a 144-pin glass epoxy substrate.

Each IC Tower consists of two 16M x 8 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP II monolithic packages. The IC Tower stacking technology is patented by STEC, Patent Number RE.36,916.

A serial EEPROM using the two pin I²C protocol is also mounted to provide the Serial Presence Detects (SPD). Decoupling capacitors of 0.1 μ F are mounted. Damping resistors are mounted for the data lines. A PLL supplies clocks to the SDRAMs from one clock input.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V. See *Ordering Information* for PC133 performance options.

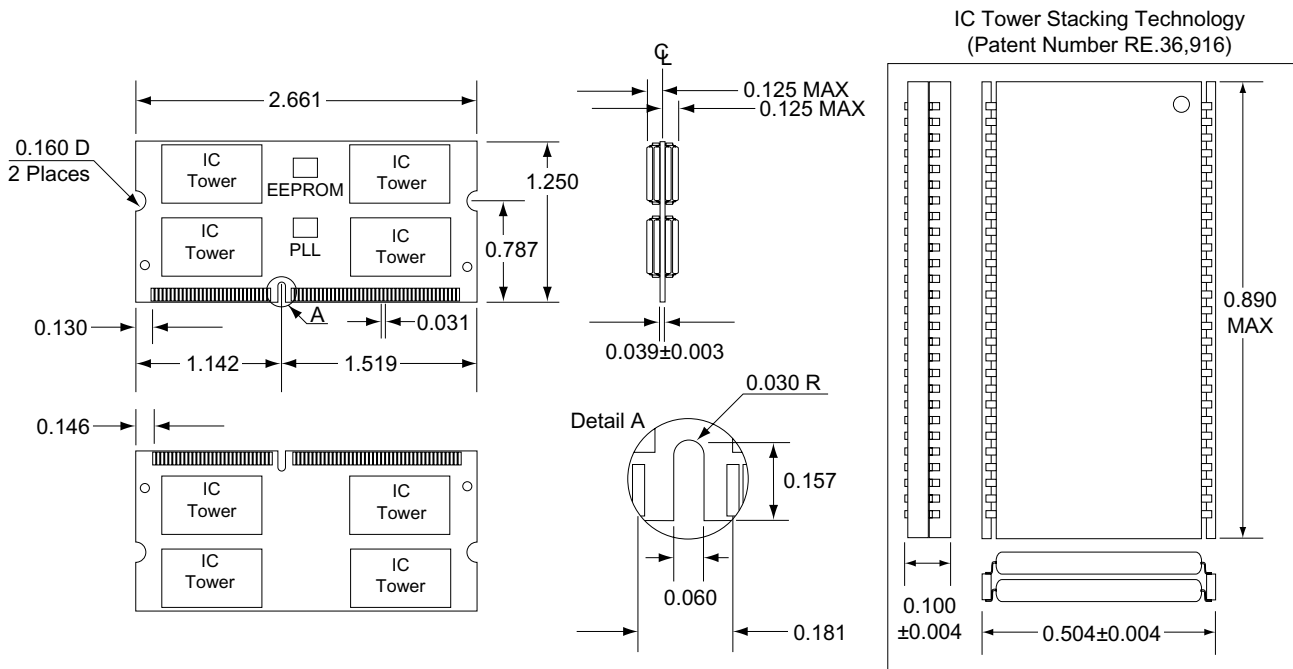
ORDERING INFORMATION

Part Number	PC133 133MHz Parameters			
	CL	tRCD	tRP	tRC
SL64G7M128M8G-B75AVU	3clks	20ns	20ns	66ns

Note: The "U" suffix added to the part number selects the RoHS compliant lead-free version.

PACKAGE DIMENSIONS

Units are in inches. Tolerances are ± 0.005 unless otherwise specified.



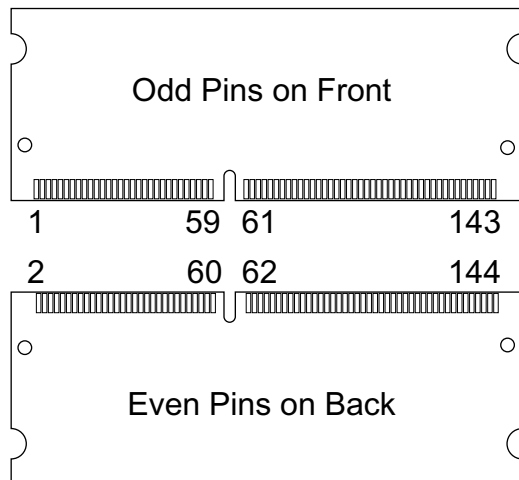
PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	21	VSS	41	DQ10	61	CLK0	81	VDD	101	VDD	121	DQ24	141	SDA
2	VSS	22	VSS	42	DQ42	62	CKE0	82	VDD	102	VDD	122	DQ56	142	SCL
3	DQ0	23	DQMB0	43	DQ11	63	VDD	83	DQ16	103	A6	123	DQ25	143	VDD
4	DQ32	24	DQMB4	44	DQ43	64	VDD	84	DQ48	104	A7	124	DQ57	144	VDD
5	DQ1	25	DQMB1	45	VDD	65	\overline{RAS}	85	DQ17	105	A8	125	DQ26		
6	DQ33	26	DQMB5	46	VDD	66	\overline{CAS}	86	DQ49	106	BA0	126	DQ58		
7	DQ2	27	VDD	47	DQ12	67	\overline{WE}	87	DQ18	107	VSS	127	DQ27		
8	DQ34	28	VDD	48	DQ44	68	CKE1	88	DQ50	108	VSS	128	DQ59		
9	DQ3	29	A0	49	DQ13	69	$\overline{S}0$	89	DQ19	109	A9	129	VDD		
10	DQ35	30	A3	50	DQ45	70	A12	90	DQ51	110	BA1	130	VDD		
11	VDD	31	A1	51	DQ14	71	$\overline{S}1$	91	VSS	111	A10/AP	131	DQ28		
12	VDD	32	A4	52	DQ46	72	A13*	92	VSS	112	A11	132	DQ60		
13	DQ4	33	A2	53	DQ15	73	NC	93	DQ20	113	VDD	133	DQ29		
14	DQ36	34	A5	54	DQ47	74	CLK1*	94	DQ52	114	VDD	134	DQ61		
15	DQ5	35	VSS	55	VSS	75	VSS	95	DQ21	115	DQMB2	135	DQ30		
16	DQ37	36	VSS	56	VSS	76	VSS	96	DQ53	116	DQMB6	136	DQ62		
17	DQ6	37	DQ8	57	CB0*	77	CB2*	97	DQ22	117	DQMB3	137	DQ31		
18	DQ38	38	DQ40	58	CB4*	78	CB6*	98	DQ54	118	DQMB7	138	DQ63		
19	DQ7	39	DQ9	59	CB1*	79	CB3*	99	DQ23	119	VSS	139	VSS		
20	DQ39	40	DQ41	60	CB5*	80	CB7*	100	DQ55	120	VSS	140	VSS		

* Not used

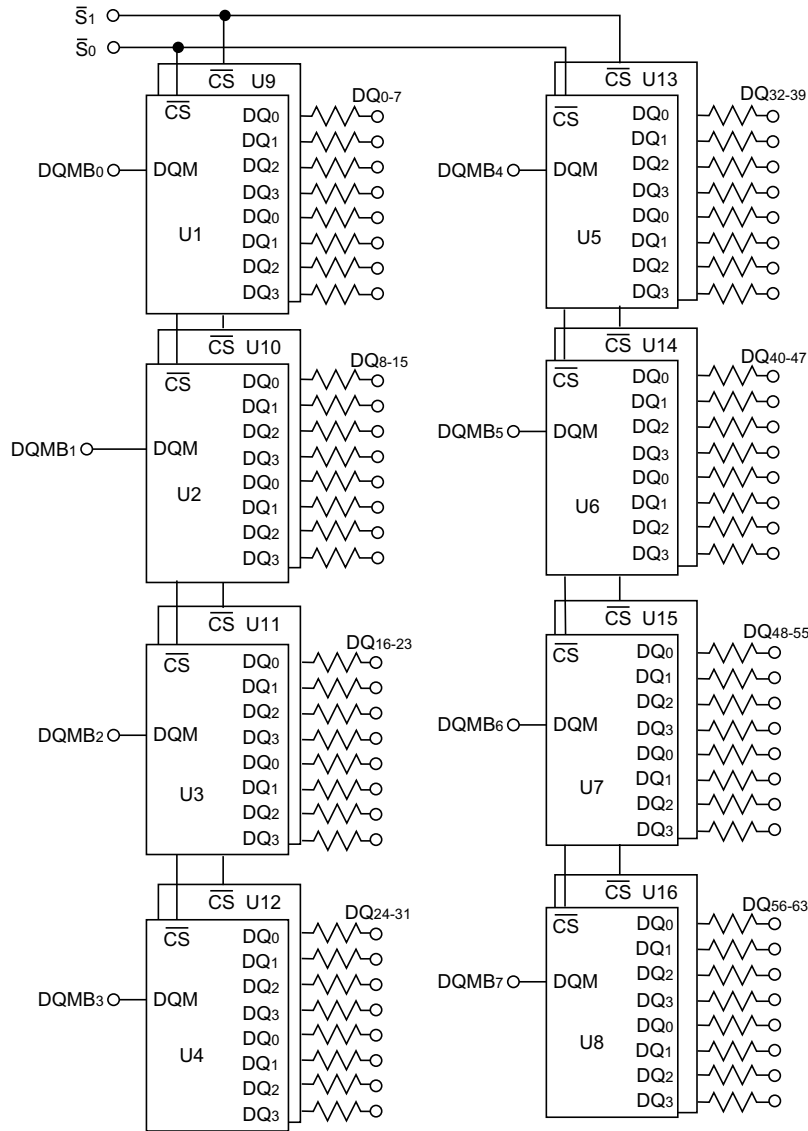
Pin Arrangement



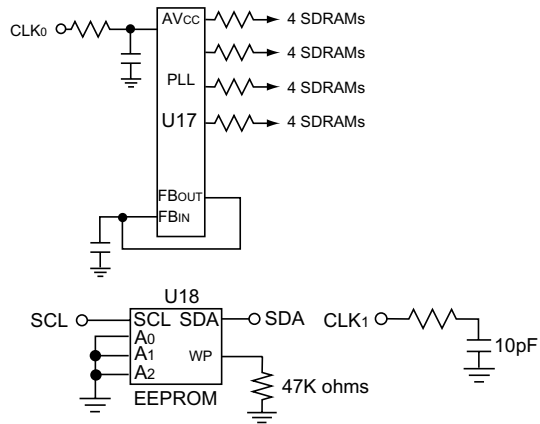
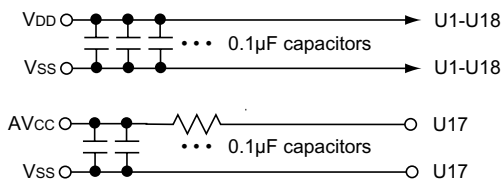
Pin Functions

Pin Name	Pin Function
A0-A10/AP, A11, A12	Address Inputs (multiplexed)
BA0, BA1	Select Bank
DQ0-DQ63	Data In/Out
\overline{WE}	Read/Write Enable
CLK0	Clock Input
CKE0, CKE1	Clock Enable Input
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
DQMB0-DQMB7	Data Input/Output Mask
$\overline{S}0, \overline{S}1$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



- A0-A10/AP, A11, A12 \rightarrow A0-A10/AP, A11, A12: SDRAMs U1-U16
- BA0, BA1 \rightarrow BA0, BA1: SDRAMs U1-U16
- $\overline{\text{RAS}}$ \rightarrow $\overline{\text{RAS}}$: SDRAMs U1-U16
- $\overline{\text{CAS}}$ \rightarrow $\overline{\text{CAS}}$: SDRAMs U1-U16
- $\overline{\text{WE}}$ \rightarrow $\overline{\text{WE}}$: SDRAMs U1-U16
- CKE0 \rightarrow CKE: SDRAMs U1-U8
- CKE1 \rightarrow CKE: SDRAMs U9-U16



Note: All resistors are 10 ohms unless otherwise specified.

SERIAL PRESENCE DETECT INFORMATIONSerial PD Interface Protocol: I²C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	SDRAM	04h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	11	0Bh
5	# of module banks on this assembly	2 banks	02h
6	Data width of this assembly	64 bits	40h
7	...Data width of this assembly (continued)	—	00h
8	Voltage interface standard of this assembly	LVTTTL	01h
9	SDRAM cycle time at CL=3 (t _{CYC})	7.5ns	75h
10	SDRAM access time from clock at CL=3 (t _{AC})	5.4ns	54h
11	DIMM configuration type	None	00h
12	Refresh rate/type	7.8μs, Self-refresh	82h
13	SDRAM width	8 bits	08h
14	Error Checking DRAM data width	None	00h
15	Min. CLK delay for back-to-back rand. col. addr.	t _{CCD} =1 CLK	01h
16	SDRAM device attributes: burst lengths supported	1,2,4,8, and Full Page	8Fh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2,3	06h
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 0	01h
21	SDRAM module attributes	on-card PLL, non-buff., non-reg.	04h
22	SDRAM device attributes: general	V _{CC} 10%, B/R, S/W, P/A, A/P	0Eh
23	Minimum clock cycle time at CL=2 (t _{CYC})	10ns	A0h
24	Max. data access time form clock at CL=2 (t _{AC})	6ns	60h
25	Minimum clock cycle time at CL=1 (t _{CYC})	—	00h
26	Max. data access time from clock at CL=1 (t _{AC})	—	00h
27	Minimum row precharge time (t _{RP})	20ns	14h
28	Minimum row active to row active delay (t _{RRD})	15ns	0Fh
29	Mininum RAS to CAS (t _{RCD})	20ns	14h
30	Mininum RAS pulse width (t _{RAS})	45ns	2Dh
31	Module bank density	512MB	80h
32	Min. command and address signal setup time (t _{AS})	1.5ns	15h
33	Min. command and address signal hold time (t _{AH})	0.8ns	08h
34	Min. data signal input setup time (t _{DS})	1.5ns	15h

(Serial Presence Detect Information continued on the next page)

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte #	Function Described	Function Supported	Hex Value
35	Min. data signal input hold time (t _{DH})	0.8ns	08h
36-61	Superset information (may be used in future)	—	00h
62	SPD revision	1.2	12h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71			00h
72	Manufacturing location	STEC USA	01h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)	01h
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	w w
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-125	Manufacturer's specific data		xxh
126	Intel specification frequency	100MHz	64h
127	Intel specification details	Detailed 100MHz Info	8Fh

ABSOLUTE MAXIMUM RATINGS¹

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to VSS	V _{IN} , V _{OUT}	-1.0 to +4.6	V
Voltage on VCC Supply Relative to VSS	V _{DD}	-1.0 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	16	W
Short Circuit Output Current	I _{OS}	50	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to VSS=0, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V _{DD}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	0	0.8	V	2
Output High Voltage Level	V _{OH}	2.4	—	—	V	3
Output Low Voltage Level	V _{OL}	—	—	0.4	V	4
Input Leakage Current	I _{IL}	-160	—	160	μA	5

1. V_{IH}(max)=5.6 V AC (pulse width ≤3 ns acceptable)
2. V_{IL}(min) = -2.0 V AC (pulse width ≤3 ns acceptable)
3. I_{OH}=-2mA for Samsung parts; I_{OH}=-4mA for Micron parts
4. I_{OOL}=2mA for Samsung parts; I_{OL}=4mA for Micron parts
5. Any input 0 ≤ V_{IN} ≤ V_{DD}.

CAPACITANCE (T_A=23 °C, V_{DD}=3.3V, f=1MHz, V_{REF}=1.4±200mA)

Item	Symbol	Max	Units
Input Capacitance (A ₀ -A ₁₀ /AP, A ₁₁ , A ₁₂ , BA ₀ , BA ₁)	C _{IN1}	71	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{WE})	C _{IN2}	71	pF
Input Capacitance (CLK ₀)	C _{IN3}	12	pF
Input Capacitance (CKE ₀ , CKE ₁)	C _{IN4}	41	pF
Input Capacitance ($\overline{S_0}$, $\overline{S_1}$)	C _{IN5}	41	pF
Input Capacitance (DQMB ₀ -DQMB ₇)	C _{IN6}	18	pF
Input/Output Capacitance (DQ ₀ -DQ ₆₃)	C _{IO1}	22	pF

DC CHARACTERISTICSRecommended operating conditions unless otherwise noted. $T_A = 0$ to 70°C .

Parameter	Symbol	Test Condition	Max	Units
Operating Current (One Bank Active)	ICC1S	Burst length=1, $t_{RC} \geq t_{RC}(\text{min})$, $I_{OL}=0\text{mA}$, Outputs open	2000	mA
Precharge Standby Current in Power-Down Mode	ICC2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CLK}=10\text{ns}$,	96	mA
	ICC2PS	CKE and $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CLK}=\text{infinity}$	80	mA
Precharge Standby Current in Non Power-Down Mode	ICC2N	CKE and $S \geq V_{IH}(\text{min})$, $t_{CLK}=10\text{ns}$ Input signals are changed one time during 20ns	480	mA
	ICC2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CLK}=\text{infinity}$ Input signals are stable	160	mA
Active Standby Current in Power-Down Mode	ICC3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CLK}=10\text{ns}$	160	mA
	ICC3PS	CKE and $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CLK}=\text{infinity}$	128	mA
Active Standby Current in Non Power-Down Mode (One Bank Active)	ICC3N	CKE and $S \geq V_{IH}(\text{min})$, $t_{CLK}=10\text{ns}$, Input signals are changed one time during 20ns	800	mA
	ICC3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CLK}=\text{infinity}$ Inputs are stable	560	mA
Operating Current (Burst Mode)	ICC4	$I_{OL}=0\text{mA}$, $\text{BL}=\text{Full Page}$, 4 banks activated $\text{ICCD}=2$ CLKs, Outputs open	2000	mA
Refresh Current (Refresh Period is 64ms)	ICC5	$t_{RC} \geq t_{RC}(\text{min})$	3040	mA
Self Refresh Current	ICC6	$\text{CKE} \leq 0.2\text{V}$	112	mA

AC TIMING PARAMETERS (TA=0-65°C; VCC=3.0V-3.6V; CL=2, 3)

Parameter	Symbol	Speed Grade 100MHz		Speed Grade 133MHz/100MHz		Unit	Notes
		Min	Max	Min	Max		
Clock Period	tCLK	10		7.5		ns	
Clock High Time (Rated @1.5V)	tCH	3		2.5		ns	
Clock Low Time	tCL	3		2.5		ns	
Input Setup Times (Data) (Address/Command & CKE)	tSI	2 2		1.5 1.5		ns	
Input Hold Times (Data) (Address/Command & CKE)	tHI	1 1		0.8 0.8		ns	
Output Valid From Clock (CL=2; limited application; 2 banks; all outputs switching)	tAC		7.0		N/A	ns	1
Output Valid From Clock (CL=2; LVTTTL levels; Rated@50pF; all outputs switching)	tAC		6.0 (tCO=5.2)		5.4 (tCO=4.6)	ns	1
Output Valid From Clock (CL=3; LVTTTL levels; Rated@50pF; all outputs switching)	tAC		6.0 (tCO=5.2)		5.4 (tCO=4.6)	ns	1
Output Hold From Clock (Rated@50pF; 1.8ns@0pF)	tOH	3		2.7		ns	
Output Valid to Z	tOHZ	3	9	2.7	7	ns	
CAS to CAS Delay	tCCD	1		1		tCLK	
CAS Bank Delay	tCBD	1		1		tCLK	
CKE to Clock Disable	tCKE	1		1		tCLK	
RAS Precharge Time	tRP	20.0		20.0		ns	
RAS Active Time	tRAS	50		45		ns	
Active to Command Delay (RAS to CAS Delay)	tRCD	20.0		20.0		ns	
RAS to RAS Bank Activate Delay	tRRD	20		15		ns	
RAS Cycle Time	tRC	70		66		ns	
DQM to Input Data Delay	tDQD	0		0		tCLK	
Write Cmd. to Input Data Delay	tDWD	0		0		tCLK	
Mode Register Set to Active Delay	tMRD	3		3		tCLK	
Precharge to O/P in High-Z	tROH		CL		CL	tCLK	2
DQM to Data in Hi-Z for Read	tDQZ	2		2		tCLK	
DQM to Data Mask for Write	tDQM	0		0		tCLK	3
Data-In to PRE Command Period	tDPL	20		15		ns	
Data-In to ACT (PRE) Cmd Period (Auto Precharge)	tDAL	5		5		tCLK	
Power Down Mode Entry	tSB		1		1	tCLK	
Self Refresh Exit Time	tSRX	10		10		ns	4
Power Down Exit Set Up Time	tPDE	1		1		tCLK	5
Clock Stop During Self Refresh or Power Down	tCLKSTP	200		200		tCLK	6
Refresh Period (4096 refresh cycles)	tREF		64		64	ms	7
Row Refresh Cycle Time	tRFC	80.0		75.0		ns	

1. Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V.
tACN=access time with 0pF load.

2. CL=CAS Latency.

3. Data Masked on the same clock.

4. Self refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + tRC.

5. Timing is asynchronous. If tset is not met by rising edge of CLK then CKE is assumed latched on next cycle.

6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.

7. For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit and 512 Mbit technology, 8192 refresh cycles.

REVISION HISTORY

Rev. **Change Description from Previous Revision**

- 101 12/10/2003. Initial release.
- 102 08/07/2007. Updated logo, web address and SPD.
- 103 08/24/2007. U added to part number.