*4M X 64 Bits (32MB) 144-Pin SDRAM Unbuffered SO-DIMM (PC100) 1 Rank x 16*

## FEATURES

- PC100 Compliant ($t_{CYC}$ = 10ns@CL = 2, 3)
- Burst Mode Operation
- Auto and self refresh capability (4096 cycles/64ms refresh)
- LVTTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (access from column address)
  - Burst Length (1, 2, 4, 8, and full page)
  - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- RoHS compliant lead-free and Industrial Operating Temperature versions available

## GENERAL DESCRIPTION

The SL64G6D4M4G-B10DV(W)(U) is a 4M x 64 bit (32MB) Synchronous Dynamic RAM (SDRAM) Small Outline Dual In-line Memory Module (SO-DIMM).

The module consists of four 1M x 16 bit x 4 bank SDRAMs in 54-pin 400-mil TSOP II packages mounted on a 144-pin glass epoxy substrate and organized in 1 rank.

A serial EEPROM using the two pin $I^2C$ protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors are mounted across the power supply. Damping resistors are mounted in series on the data lines.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V and unbuffered signals.

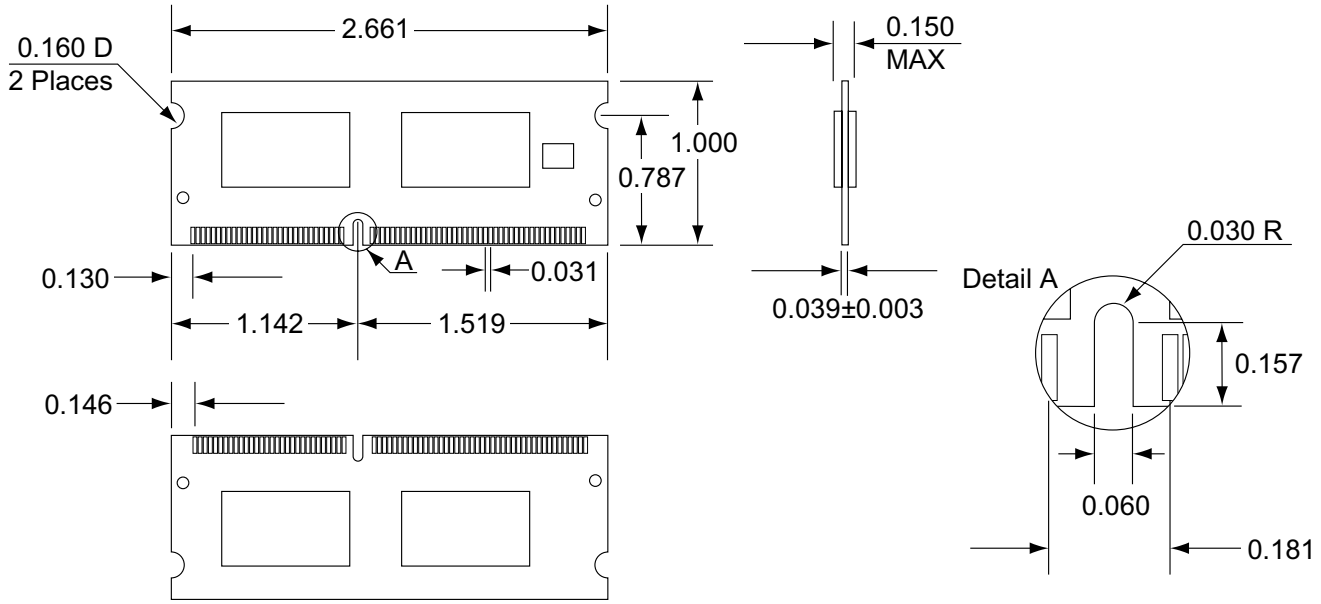
## ORDERING INFORMATION

| Part Number | $t_{CYC}$ | CL | $t_{RCD}$ | $t_{RP}$ | $t_{RC}$ | Comment |
|---|---|---|---|---|---|---|
| SL64G6D4M4G-B10DV(W)(U) | 10ns | 2clks | 2clks | 2clks | 7clks | PC100 |

Notes:
1. A "W" in the suffix of the part number selects the Industrial Operating Temperature Range version of the module ($T_A$= -40 to 85°C). This version is built with Industrial Temperature SDRAMs.
2. The "U" in the part number selects the RoHS Compliant, lead-free version of the module.

## PACKAGE DIMENSIONS

Units are in inches. Tolerances are ±0.005 unless otherwise specified.



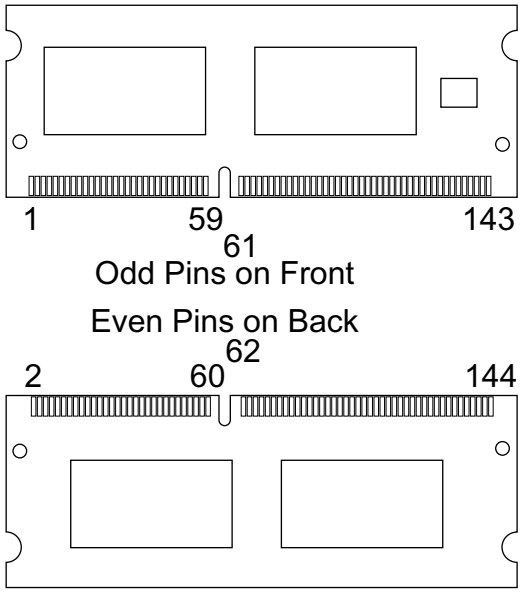
# PIN CONFIGURATION

## Pin Symbols

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 21 | $V_{SS}$ | 41 | $DQ_{10}$ | 61 | $CLK_0$ | 81 | $V_{DD}$ | 101 | $V_{DD}$ | 121 | $DQ_{24}$ | 141 | SDA |
| 2 | $V_{SS}$ | 22 | $V_{SS}$ | 42 | $DQ_{42}$ | 62 | $CKE_0$ | 82 | $V_{DD}$ | 102 | $V_{DD}$ | 122 | $DQ_{56}$ | 142 | SCL |
| 3 | $DQ_0$ | 23 | $DQMB_0$ | 43 | $DQ_{11}$ | 63 | $V_{DD}$ | 83 | $DQ_{16}$ | 103 | $A_6$ | 123 | $DQ_{25}$ | 143 | $V_{DD}$ |
| 4 | $DQ_{32}$ | 24 | $DQMB_4$ | 44 | $DQ_{43}$ | 64 | $V_{DD}$ | 84 | $DQ_{48}$ | 104 | $A_7$ | 124 | $DQ_{57}$ | 144 | $V_{DD}$ |
| 5 | $DQ_1$ | 25 | $DQMB_1$ | 45 | $V_{DD}$ | 65 | $\overline{RAS}$ | 85 | $DQ_{17}$ | 105 | $A_8$ | 125 | $DQ_{26}$ | | |
| 6 | $DQ_{33}$ | 26 | $DQMB_5$ | 46 | $V_{DD}$ | 66 | $\overline{CAS}$ | 86 | $DQ_{49}$ | 106 | $BA_0$ | 126 | $DQ_{58}$ | | |
| 7 | $DQ_2$ | 27 | $V_{DD}$ | 47 | $DQ_{12}$ | 67 | $\overline{WE}$ | 87 | $DQ_{18}$ | 107 | $V_{SS}$ | 127 | $DQ_{27}$ | | |
| 8 | $DQ_{34}$ | 28 | $V_{DD}$ | 48 | $DQ_{44}$ | 68 | $CKE_1$* | 88 | $DQ_{50}$ | 108 | $V_{SS}$ | 128 | $DQ_{59}$ | | |
| 9 | $DQ_3$ | 29 | $A_0$ | 49 | $DQ_{13}$ | 69 | $\overline{S}_0$ | 89 | $DQ_{19}$ | 109 | $A_9$ | 129 | $V_{DD}$ | | |
| 10 | $DQ_{35}$ | 30 | $A_3$ | 50 | $DQ_{45}$ | 70 | $A_{12}$* | 90 | $DQ_{51}$ | 110 | $BA_1$ | 130 | $V_{DD}$ | | |
| 11 | $V_{DD}$ | 31 | $A_1$ | 51 | $DQ_{14}$ | 71 | $\overline{S}_1$* | 91 | $V_{SS}$ | 111 | $A_{10}$/AP | 131 | $DQ_{28}$ | | |
| 12 | $V_{DD}$ | 32 | $A_4$ | 52 | $DQ_{46}$ | 72 | $A_{13}$* | 92 | $V_{SS}$ | 112 | $A_{11}$ | 132 | $DQ_{60}$ | | |
| 13 | $DQ_4$ | 33 | $A_2$ | 53 | $DQ_{15}$ | 73 | NC | 93 | $DQ_{20}$ | 113 | $V_{DD}$ | 133 | $DQ_{29}$ | | |
| 14 | $DQ_{36}$ | 34 | $A_5$ | 54 | $DQ_{47}$ | 74 | $CLK_1$ | 94 | $DQ_{52}$ | 114 | $V_{DD}$ | 134 | $DQ_{61}$ | | |
| 15 | $DQ_5$ | 35 | $V_{SS}$ | 55 | $V_{SS}$ | 75 | $V_{SS}$ | 95 | $DQ_{21}$ | 115 | $DQMB_2$ | 135 | $DQ_{30}$ | | |
| 16 | $DQ_{37}$ | 36 | $V_{SS}$ | 56 | $V_{SS}$ | 76 | $V_{SS}$ | 96 | $DQ_{53}$ | 116 | $DQMB_6$ | 136 | $DQ_{62}$ | | |
| 17 | $DQ_6$ | 37 | $DQ_8$ | 57 | NC | 77 | NC | 97 | $DQ_{22}$ | 117 | $DQMB_3$ | 137 | $DQ_{31}$ | | |
| 18 | $DQ_{38}$ | 38 | $DQ_{40}$ | 58 | NC | 78 | NC | 98 | $DQ_{54}$ | 118 | $DQMB_7$ | 138 | $DQ_{63}$ | | |
| 19 | $DQ_7$ | 39 | $DQ_9$ | 59 | NC | 79 | NC | 99 | $DQ_{23}$ | 119 | $V_{SS}$ | 139 | $V_{SS}$ | | |
| 20 | $DQ_{39}$ | 40 | $DQ_{41}$ | 60 | NC | 80 | NC | 100 | $DQ_{55}$ | 120 | $V_{SS}$ | 140 | $V_{SS}$ | | |

* Not used

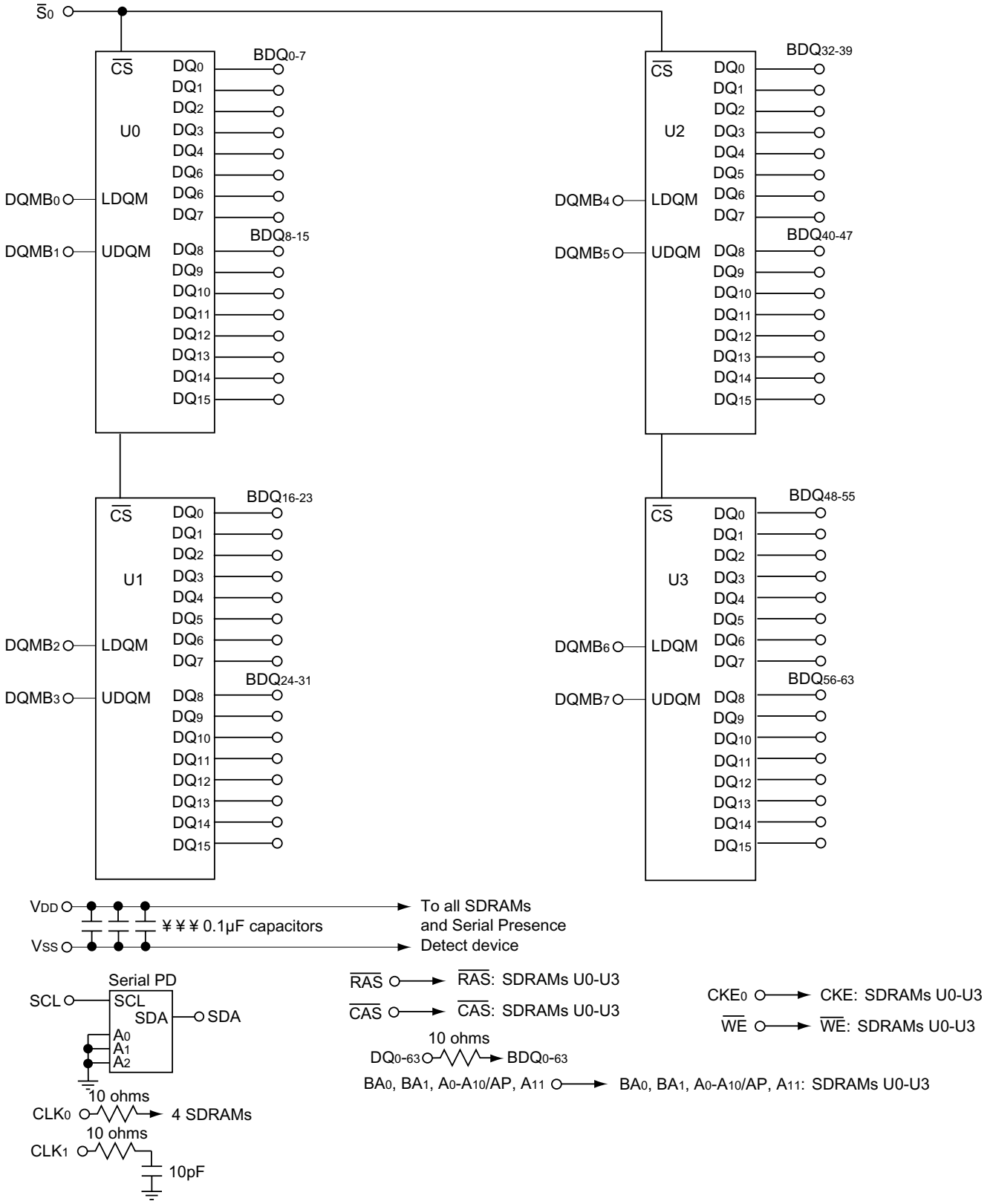
## Pin Arrangement




## Pin Functions

| Pin Name | Pin Function |
|---|---|
| $A_0$-$A_{10}$/AP, $A_{11}$ | Address Inputs (multiplexed) |
| $BA_0$, $BA_1$ | Select Bank |
| $DQ_0$-$DQ_{63}$ | Data In/Out |
| $\overline{WE}$ | Read/Write Enable |
| $CLK_0$, $CLK_1$ | Clock Input |
| $CKE_0$ | Clock Enable Input |
| $\overline{RAS}$ | Row Adress Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $DQMB_0$-$DQMB_7$ | Data Input/Output Mask |
| $\overline{S}_0$ | Chip Select Input |
| SDA | Serial Data I/O |
| SCL | Serial Clock |
| $V_{DD}$ | Power (+3.3V) |
| $V_{SS}$ | Ground |
| NC | No Connection |

## FUNCTIONAL BLOCK DIAGRAM



## SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: $I^2C$; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

| Byte # | Function Described | Function Supported | Hex Value |
|---|---|---|---|
| 0 | # of bytes written into serial memory at module manufacturer | 128 bytes | 80h |
| 1 | Total # of bytes of SPD memory device | 256Bytes (2K-bit) | 08h |
| 2 | Fundamental memory type | SDRAM | 04h |
| 3 | # of row addresses on this assembly | 12 | 0Ch |
| 4 | # of column addresses on this assembly | 8 | 08h |
| 5 | # of module ranks on this assembly | 1 rank | 01h |
| 6 | Data width of this assembly | 64 bits | 40h |
| 7 | …Data width of this assembly (continued) | — | 00h |
| 8 | Voltage interface standard of this assembly | LVTTL | 01h |
| 9 | SDRAM cycle time at CL=3 ($t_{CYC}$) | 10ns | A0h |
| 10 | SDRAM access time from clock at CL=3 ($t_{AC}$) | 6ns | 60h |
| 11 | DIMM configuration type | non-ECC | 00h |
| 12 | Refresh rate/type | 15.625µs, Self-refresh | 80h |
| 13 | SDRAM width | 16 bits | 10h |
| 14 | Error Checking DRAM data width | none | 00h |
| 15 | Min. CLK delay for back-to-back rand. col. addr. | $t_{CCD}$=1 CLK | 01h |
| 16 | SDRAM device attributes: burst lengths supported | 1,2,4,8, and full page | 8Fh |
| 17 | SDRAM device attributes: # of banks on SDRAM device | 4 banks | 04h |
| 18 | SDRAM device attributes: CAS latency | CAS latency = 2,3 | 06h |
| 19 | SDRAM device attributes: CS latency | CS latency = 0 | 01h |
| 20 | SDRAM device attributes: Write latency | Write Latency = 0 | 01h |
| 21 | SDRAM module attributes | non-buff., non-reg., non-PLL | 00h |
| 22 | SDRAM device attributes: general | $V_{CC}$10%, B/R, S/W, P/A, A/P | 0Eh |
| 23 | Minimum clock cycle time at CL=2 ($t_{CYC}$) | 10ns | A0h |
| 24 | Max. data access time form clock at CL=2 ($t_{AC}$) | 6ns | 60h |
| 25 | Minimum clock cycle time at CL=1 ($t_{CYC}$) | — | 00h |
| 26 | Max. data access time from clock at CL=1 ($t_{AC}$) | — | 00h |
| 27 | Minimum row precharge time ($t_{RP}$) | 20ns | 14h |
| 28 | Minimum row active to row active delay ($t_{RRD}$) | 20ns | 14h |
| 29 | Minumum RAS to CAS ($t_{RCD}$) | 20ns | 14h |
| 30 | Minumum RAS pulse width ($t_{RAS}$) | 50ns | 32h |
| 31 | Module bank density | 32MB | 08h |
| 32 | Min. command and address signal setup time ($t_{AS}$) | 2ns | 20h |
| 33 | Min. command and address signal hold time ($t_{AH}$) | 1ns | 10h |
| 34 | Min. data signal input setup time ($t_{DS}$) | 2ns | 20h |

*(Serial Presence Detect Information continued on the next page)*

## SERIAL PRESENCE DETECT INFORMATION *(continued)*

| Byte # | Function Described | Function Supported | Hex Value |
|---|---|---|---|
| 35 | Min. data signal input hold time ($t_{DH}$) | 1ns | 10h |
| 36-61 | Superset information (may be used in future) | — | 00h |
| 62 | SPD revision | JEDEC revision 1.2 | 12h |
| 63 | Checksum for bytes 0-62 | JEDEC calculation | xxh |
| 64 | Manufacturer's JEDEC ID code per JEP-106E | Continuation code | 7Fh |
| 65 | Man. JEDEC ID code (continued) | STEC's ID | A8h |
| 66-71 | | | 00h |
| 72 | Manufacturing location | STEC USA<br>or STEC Malaysia | 01h (USA)<br>or 02h |
| 73-90 | Manufacturer's part number | | xxh |
| 91 | Revision code of PCB | RevA(01),RevB(02) | xxh |
| 92 | | | 00h |
| 93 | Manufacturing date | Year (BCD) | yy |
| 94 | | Calender Week (BCD) | w w |
| 95 | Assembly serial number | Tester number | ss |
| 96 | | Serial number (bits 7-0) | ss |
| 97 | | Serial number (bits 15-8) | ss |
| 98 | | Serial number (bits 23-16) | ss |
| 99-125 | Manufacturer's specific data | | xxh |
| 126 | Intel specification frequency | 100MHz | 64h |
| 127 | Intel specification details | CLK0; junc temp.TBD;<br>CL2,CL3; concurrent AP | 8Fh |
| 128+ | — | | 00h |

## ABSOLUTE MAXIMUM RATINGS[1]

| Item | Symbol | Rating | Units |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -1.0 to +4.6 | V |
| Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ | $V_{DD}$ | -1.0 to +4.6 | V |
| Storage Temperature | $T_{stg}$ | -55 to +150 | °C |
| Power Dissipation | $P_D$ | 4 | W |
| Short Circuit Output Current | $I_{OS}$ | 50 | mA |

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltage reference to $V_{SS}$=0)

| Item | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Commercial Operating Temperature Range<br>Industrial Operating Temperature Range | $T_A$<br>$T_A$ | 0<br>–40 | 25 | 70<br>85 | °C<br>°C | |
| Supply Voltage | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | 3.0 | $V_{DD}$+0.3 | V | 1 |
| Input Low Voltage | $V_{IL}$ | –0.3 | 0 | 0.8 | V | 2 |
| Output High Voltage Level | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$= –4mA |
| Output Low Voltage Level | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$=4mA |
| Input Leakage Current | $I_{IL}$ | -20 | — | 20 | µA | 3 |
| Output Leakage Current | $I_{OL}$ | -5 | | 5 | | 3, 4 |

1. $V_{IH}$(max)=5.6 V AC (pulse width <=3 ns acceptable).
2. $V_{IL}$(min) = -2.0 V AC (pulse width <=3 ns acceptable).
3. Any input 0<=$V_{IN}$<=$V_{DD}$.
4. Data out is disabled, 0<=$V_{OUT}$<=$V_{DD}$.

## CAPACITANCE ($T_A$=25°C, $V_{DD}$=3.3V, f=1MHz, $V_{REF}$=1.4±200mA)

| Item | Symbol | Max | Units |
|---|---|---|---|
| Input Capacitance ( A, BA, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)<br>20pF adder for board. | $C_{IN1}$ | 40 | pF |
| Input Capacitance (CKE)<br>20pF adder for board. | $C_{IN2}$ | 40 | pF |
| Input Capacitance ($\overline{S}$)<br>20pF adder for board. | $C_{IN3}$ | 40 | pF |
| Input Capacitance (CLK)<br>10pF adder for board. | $C_{IN4}$ | 26 | pF |
| Input Capacitance (DQMB)<br>5pF adder for board. | $C_{IN5}$ | 10 | pF |
| Input/Output Capacitance (DQ)<br>5pF adder for board. | $C_{IO1}$ | 11.5 | pF |

## DC CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

| Parameter/Condition | Symbol | Max | Units | Notes |
|---|---|---|---|---|
| OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; tRC >= tRC (MIN) | IDD1 | 460 | mA | 1,3,4,5,6 |
| STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW | IDD2 | 8 | mA | 5 |
| STANDBY CURRENT: Active Mode; CKE = HIGH; CS = HIGH; All banks active after tRCD met; No accesses in progress | IDD3 | 180 | mA | 1,2,4,5,6 |
| OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active | IDD4 | 560 | mA | 1,3,4,5,6 |
| AUTO REFRESH CURRENT: tRFC = tRFC (MIN) CKE = HIGH; CS = HIGH | IDD5 | 840 | mA | 1,2,3,4,5,6 |
| SELF REFRESH CURRENT: Standard CKE <= 0.2V | IDD7 | 4 | mA | |

1. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
2. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
3. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. For CL=2 and tCK=10ns.
6. For modules with more than one rank, IDDn is specified with one rank in IDDn and the other ranks in IDD2, where n is IDD number in the Symbol column.

## AC TIMING PARAMETERS *(Recommended operating conditions unless otherwise specified.)*

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock Period CL3<br>CL2 | $t_{CLK}$ | 10<br>10 | | ns<br>ns | |
| Clock High Time (Rated @1.5V) | $t_{CH}$ | 3 | | ns | |
| Clock Low Time | $t_{CL}$ | 3 | | ns | |
| Input Setup Times (Data)<br>(Address/Command & CKE) | $t_{SI}$ | 2<br>2 | | ns<br>ns | |
| Input Hold Times (Data)<br>(Address/Command & CKE) | $t_{HI}$ | 1<br>1 | | ns<br>ns | |
| Output Valid From Clock CL3<br>(LVTTL levels; Rated@50pF; CL2<br>all outputsswitching) | $t_{AC}$ | | 6<br>6 | ns<br>ns | 1<br>1 |
| Output Hold From Clock (Rated@50pF) | $t_{OH}$ | 3 | | ns | |
| CAS to CAS Delay | $t_{CCD}$ | 1 | | $t_{CLK}$ | |
| CKE to Clock Disable | $t_{CKE}$ | 1 | | $t_{CLK}$ | |
| RAS Precharge Time | $t_{RP}$ | 2 | | $t_{CLK}$ | |
| RAS Active Time | $t_{RAS}$ | 5 | 12K | $t_{CLK}$ | |
| Active to Command Delay (RAS to CAS Delay) | $t_{RCD}$ | 2 | | $t_{CLK}$ | |
| RAS to RAS Bank Activate Delay | $t_{RRD}$ | 2 | | $t_{CLK}$ | |
| RAS Cycle Time | $t_{RC}$ | 7 | | $t_{CLK}$ | |
| DQM to Input Data Delay | $t_{DQD}$ | 0 | | $t_{CLK}$ | |
| Write Cmd. to Input Data Delay | $t_{DWD}$ | 0 | | $t_{CLK}$ | |
| Mode Register Set to Active Delay | $t_{MRD}$ | 3 | | $t_{CLK}$ | |
| Precharge to O/P in High-Z | $t_{ROH}$ | | CL | $t_{CLK}$ | 2 |
| DQM to Data in Hi-Z for Read | $t_{DQZ}$ | 2 | | $t_{CLK}$ | |
| DQM to Data Mask for Write | $t_{DQM}$ | 0 | | $t_{CLK}$ | 3 |
| Data-In to PRE Command Period | $t_{DPL}$ | 2 | | 2tCLK | |
| Data-In to ACT (PRE) Cmd Period (Auto Precharge) | $t_{DAL}$ | 5 | | $t_{CLK}$ | |
| Power Down Mode Entry | $t_{SB}$ | | 1 | $t_{CLK}$ | |
| Exti Self Refresh to Active Time | $t_{XSR}$ | 1 | | $t_{CLK}$ | |
| Power Down Exit Set Up Time | $t_{PDE}$ | 1 | | $t_{CLK}$ | 4 |
| Clock Stop During Self Refresh or Power Down | $t_{CLKSTP}$ | 200 | | $t_{CLK}$ | 5 |
| Refresh Period | $t_{REF}$ | | 64 | ms | 6 |

1. Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V. $t_{ACN}$=access time with 0pF load.
2. CL=CAS Latency.
3. Data Masked on the same clock.
4. Timing is asynchronous. If $t_{set}$ is not met by rising edge of CLK then CKE is assumed latched on next cycle.
5. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
6. For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit and 512Mbit technology, 8192 refresh cycles.

## REVISION HISTORY

| Rev. | Change Description from Previous Revision |
|---|---|
| -102 | 07/06/2006. Updated to current format and die revs. |
| -103 | 08/07/2007. Logo updated. |

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