

## 128M X 72 Bit (1 GB) 184-Pin Very Low Profile (VLP) Registered DDR DIMM ECC (PC3200) 1 Rank x 4

### FEATURES

- PC3200 Compliant  
(DDR400 200MHz-5ns; CL-tRCD-tRP = 3-3-3 clks)
- 184-Pin VLP RDIMM form factor
- Auto and self refresh capability  
(8192 cycles/64ms refresh)
- SSTL\_2 compatible inputs and outputs
- +2.6V ± 0.1V VDD and VDDQ
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM
- ECC
- RoHS Compliant, lead-free version available

### GENERAL DESCRIPTION

The SL72E4M128M8M-D05AW(U) is a 128M x 72 bit Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Very Low Profile (VLP) Registered Dual In-line Memory Module (RDIMM) with ECC.

This module consists of eighteen CMOS 32M x 4 bit x 4 bank DDR SDRAMs in BGA packages. The DDR SDRAMs are mounted in on a 184-pin glass epoxy substrate and organized in 1 rank.

A serial EEPROM using the two pin IIC protocol is also mounted to provide for the Serial Presence Detects (SPD). PLL circuits supply clocks to the DDR SDRAMs from one clock input. Decoupling capacitors are mounted in parallel across the power supply. Damping resistors are added in series to the DQ and DQS signals.

All control and address signals are re-driven through registers to the SDRAM devices. The control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock).

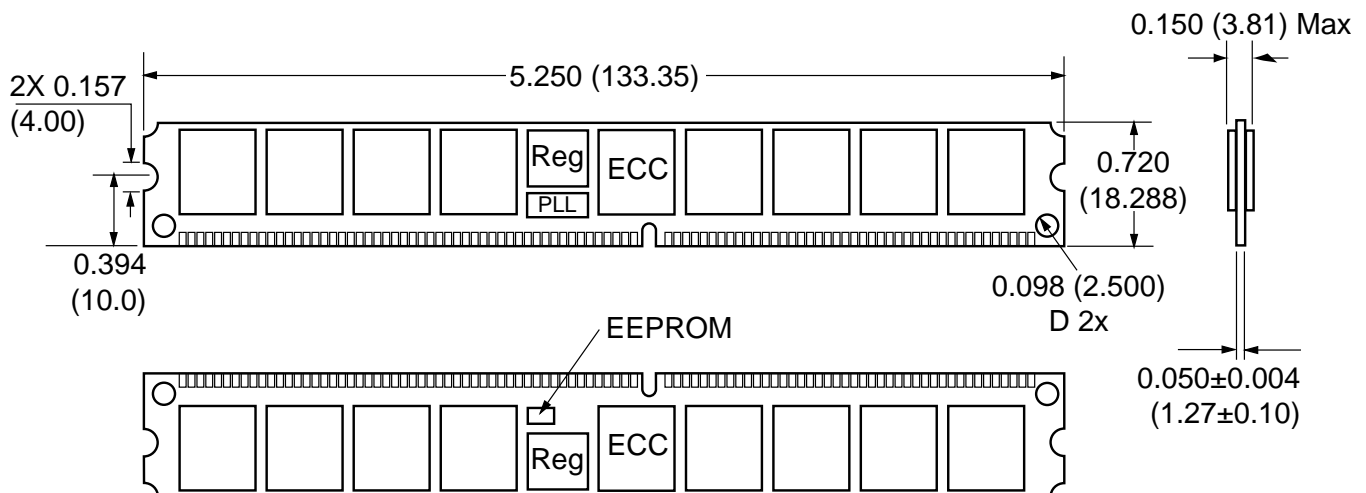
The module has gold edge connections and is intended for mounting into 184-pin RDIMM edge connector sockets keyed for 2.5V VDD and VDDQ.

### ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72E4M128M8M-D05AW(U)	3	200	3.2 GB/s
The "U" suffix added to the part number selects the RoHS Compliant, lead-free version of the module.			

### PACKAGE DIMENSIONS

Units are in inches (millimeters). Tolerances are ±0.005 (±0.127) unless otherwise specified.



(Where U selects the RoHS Compliant, lead-free version.)

## PIN CONFIGURATION (\* = Not Used; / = Active Low)

### Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	VSS	32	A5	124	VSS	62	VDDQ	154	/RAS
2	DQ0	94	DQ4	33	DQ24	125	A6	63	/WE	155	DQ45
3	VSS	95	DQ5	34	VSS	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	/CAS	157	/S0
5	DQS0	97	DQS9	36	DQS3	128	VDDQ	66	VSS	158	/S1*
6	DQ2	98	DQ6	37	A4	129	DQS12	67	DQS5	159	DQS14
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	VSS
8	DQ3	100	VSS	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	VSS	70	VDD	162	DQ47
10	/RESET	102	NC	41	A2	133	DQ31	71	/S2*	163	/S3*
11	VSS	103	FETEN*	42	VSS	134	CB4	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	CB5	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	CB0	136	VDDQ	74	VSS	166	DQS3
14	DQS1	106	DQ13	45	CB1	137	CK0	75	CK2*	167	A13*
15	VDDQ	107	DQS10	46	VDD	138	/CK0	76	/CK2*	168	VDD
16	CK1*	108	VDD	47	DQS8	139	VSS	77	VDDQ	169	DQS15
17	/CK1*	109	DQ14	48	A0	140	DQS17	78	DQS6	170	DQ54
18	VSS	110	DQ15	49	CB2	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1*	50	VSS	142	CB6	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	CB3	143	VDDQ	81	VSS	173	NC
21	CKE0	113	BA2*	52	BA1	144	CB7	82	VDDID	174	DQ60
22	VDDQ	114	DQ20		<b>Key</b>		<b>Key</b>	83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	VSS	84	DQ57	176	VSS
24	DQ17	116	VSS	54	VDDQ	146	DQ36	85	VDD	177	DQS16
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	VSS	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DQS11	57	DQ34	149	DQS13	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	VSS	150	DQ38	89	VSS	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	VDDQ	122	A8	60	DQ35	152	VSS	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

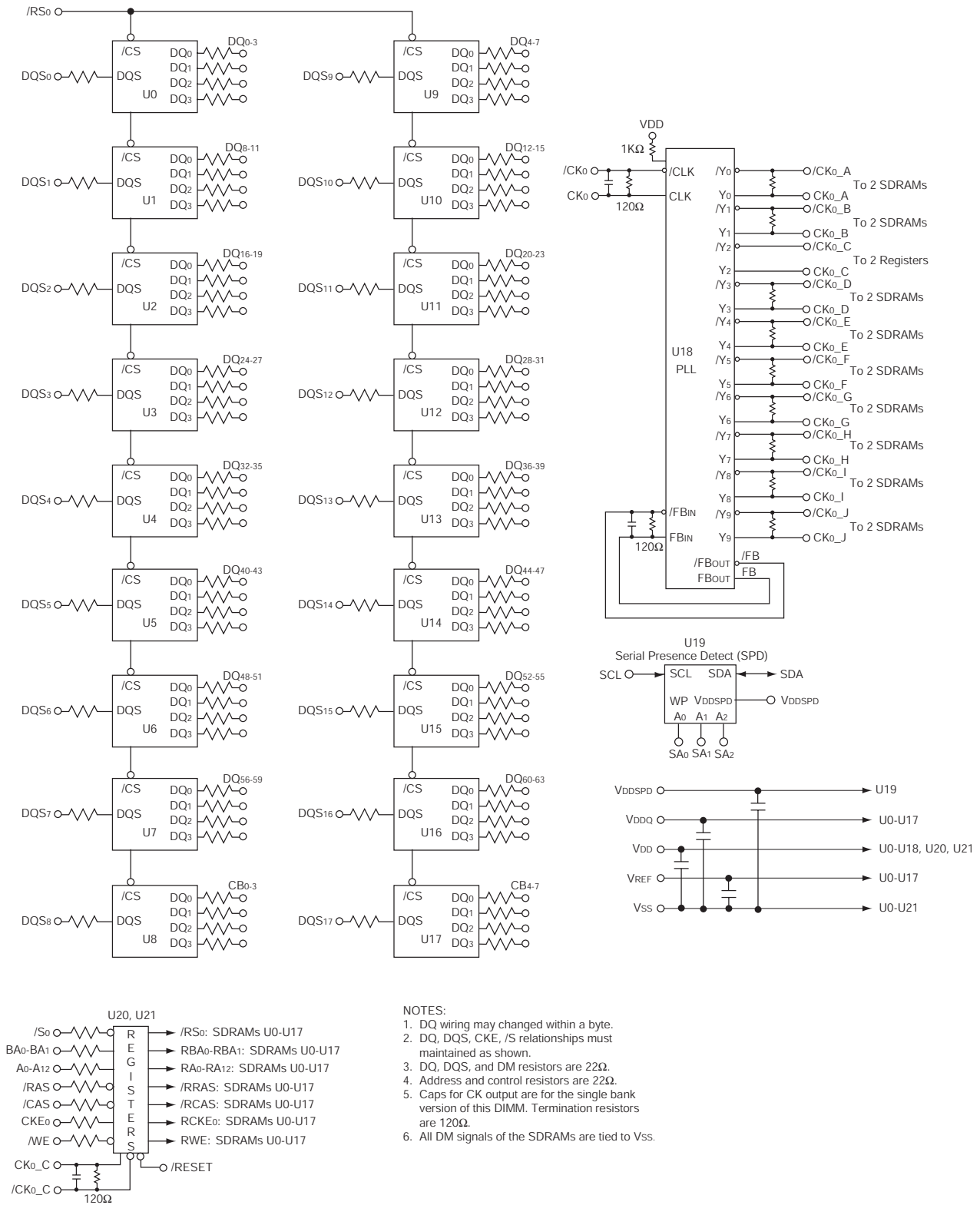
### Pin Description

Pin Symbol	Pin Description
A0-A11, A12, A13*	SDRAM address bus
BA0-BA1, BA2*	SDRAM bank select
DQ0-DQ63	DIMM memory data bus
CB0-CB7	DIMM ECC check bits
/RAS	SDRAM row address strobe
/CAS	SDRAM column address strobe
/WE	SDRAM write strobe
/S0, /S1*, /S2*, /S3*	SDRAM chip select lines (Physical ranks 0, 1, 2, and 3)
CKE0, CKE1*	SDRAM clock enable lines
DQS0-DQS17	SDRAM data strobes
CK0, CK1*, CK2*	SDRAM clock (positive line of differential pair)
/CK0, /CK1*, /CK2*	SDRAM clock (negative line of differential pair)

Pin Symbol	Pin Description
SCL	IIC serial bus clock for EEPROM
SDA	IIC serial bus data line for EEPROM
SA0-SA2	IIC slave address select for EEPROM
VDD	SDRAM positive power supply
VDDQ	SDRAM I/O driver positive power supply
VDDID	VDD Identification flag (No connect for VDD=VDDQ)
VREF	SDRAM I/O reference supply
VSS	Power supply return (ground)
VDDSPD	Serial EEPROM positive power supply (2.2V to 5.5V)
NC	Spare pins (no connect)
/RESET	Reset pin (forces register inputs low)
FETEN*	FET enable line

(Where U selects the RoHS Compliant, lead-free version.)

## FUNCTIONAL BLOCK DIAGRAM



- NOTES:**
1. DQ wiring may be changed within a byte.
  2. DQ, DQS, CKE, /S relationships must be maintained as shown.
  3. DQ, DQS, and DM resistors are 22Ω.
  4. Address and control resistors are 22Ω.
  5. Caps for CK output are for the single bank version of this DIMM. Termination resistors are 120Ω.
  6. All DM signals of the SDRAMs are tied to Vss.

*(Where U selects the RoHS Compliant, lead-free version.)***SERIAL PRESENCE DETECT INFORMATION**

Serial PD Interface Protocol: IIC; Current sink capability of SDA driver &lt;= 3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	DDR SDRAM	07h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	12	0Ch
5	# of physical ranks on this assembly	1 rank	01h
6	Data width of this assembly	72 bits	48h
7	...Data width of this assembly (continued)	—	00h
8	Voltage interface level of this assembly	SSTL 2.5V	04h
9	SDRAM cycle time at CL=3 (tCYC)	5ns	50h
10	SDRAM access time from clock at CL=3 (tAC)	0.7ns	70h
11	DIMM configuration type	ECC	02h
12	Refresh rate/type	7.8µs, Self -refresh	82h
13	SDRAM width	4 bits	04h
14	Error Checking SDRAM data width	4 bits	04h
15	Min. CLK delay for back-to-back rand. col. addr.	tCCD=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	2,4,8	0Eh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5, 3	1Ch
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 1	02h
21	SDRAM module attributes	Registered with Differential clock, PLL	26h
22	SDRAM device attributes: general	Fast/Concurrent AP	C0h
23	Minimum clock cycle time at CL=2.5 (tCYC)	6.0ns	60h
24	Max. data access time form clock at CL=2.5 (tAC)	0.7ns	70h
25	Minimum clock cycle time at CL=2 (tCYC)	7.5	75h
26	Max. data access time from clock at CL=2 (tAC)	0.75	75h
27	Minimum row precharge time (tRP)	15ns	3Ch
28	Minimum row active to row active delay (tRRD)	10ns	28h
29	Minumum RAS to CAS (tRCD)	15ns	3Ch
30	Minumum RAS pulse width (tRAS)	40ns	28h
31	Module bank density	1GB	01h
32	Min. command and address signal setup time (tIS)	0.60ns	60h
33	Min. command and address signal hold time (tIH)	0.60ns	60h
34	Min. data/data mask signal input setup time (tDS)	0.40ns	40h
35	Min. data/data mask signal input hold time (tDH)	0.40ns	40h

continued on the next page

*(Where U selects the RoHS Compliant, lead-free version.)***SERIAL PRESENCE DETECT INFORMATION** *(continued)*

Byte #	Function Described	Function Supported	Hex Value
36-40	Reserved		00h
41	Row cycle time (t <sub>RC</sub> )	55ns	37h
42	Auto refresh cycle time (t <sub>RFC</sub> )	70ns	46h
43	Maximum SDRAM device cycle time (t <sub>CK_MAX</sub> )	12ns	30h
44	DQS-DQ skew (t <sub>DQSQ</sub> )	0.40ns	28h
45	SDRAM device data hold skew factor (t <sub>QHS</sub> )	0.50ns	50h
46	Reserved		00h
47	DDR SDRAM DIMM height	No DIMM height available (0.72")	00h
48-61	Reserved		00h
62	SPD revision	JEDEC initial release	00h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71			00h
72	Manufacturing location	STEC USA/Malaysia	01h/02h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	RevA(01),RevB(02)	xxh
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	w w
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
99-127	Manufacturer's specific data		xxh
128-255	Open for Customer Use	Undefined	00h

(Where U selects the RoHS Compliant, lead-free version.)

**ABSOLUTE MAXIMUM RATINGS**

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional Operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time may affect device reliability.

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 to +3.6	V
Voltage on VDD supply relative to VSS	VDD	-1.0 to +3.6	V
Voltage on VDDQ supply relative to VSS	VDDQ	-1.0 to 3.6	V
Storage temperature	T <sub>STG</sub>	-55 to +125	°C
Power Dissipation	P <sub>D</sub>	27	W
Short circuit current	I <sub>OS</sub>	50	mA

**POWER and DC OPERATING CONDITIONS (SSTL\_2 IN/OUT)**

Recommended operating conditions (Voltage referenced to VSS=0V. T<sub>A</sub>= 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (for device with a nominal VDD of 2.6V)	VDD	2.5	2.7	V	
I/O Supply voltage	VDDQ	2.5	2.7	V	
I/O Reference voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	1
I/O Termination voltage (system)	VTT	VREF-0.04	VREF+0.04	V	2
Input logic high voltage	V <sub>IH</sub> (DC)	VREF+0.15	VDDQ+0.3	V	4
Input logic low voltage	V <sub>IL</sub> (DC)	-0.3	VREF-0.15	V	4
Input voltage level, CK and /CK	V <sub>IN</sub> (DC)	-0.3	VDDQ+0.3	V	
Input differential voltage, CK and /CK	V <sub>ID</sub> (DC)	0.36	VDDQ+0.6	V	3
Input leakage current: A, BA, /RAS, /CAS, /WE, CKE, /S (Registered) CK, /CK (PLL)	I <sub>L</sub> I <sub>L</sub>	-5 -10	5 10	μA μA	
Output leakage current: DQ, CB, DQS	I <sub>OZ</sub>	-5	5	μA	
Output high current (V <sub>OUT</sub> = VDDQ - 0.373V, minimum VREF, minimum VTT)	I <sub>OH</sub>	-16.8		mA	
Output low current (V <sub>OUT</sub> = 0.373V, maximum VREF, maximum VTT)	I <sub>OL</sub>	16.8		mA	

- Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of <= 3nH.
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
- VID is the magnitude of the difference between the input level on CK and the input level on /CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
- The value of VIX is expected to equal 0.5\*VDDQ of the transmitting device and must track variations in the dc level of the same.
- These characteristics obey the SSTL-2 class II standards.

(Where U selects the RoHS Compliant, lead-free version.)

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted. Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap. VDD=2.7V. T<sub>A</sub>=10°C)

Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; t RC = t RC (MIN); t CK = t CK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;	IDD0*	2,790	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; t RC = t RC (MIN); t CK = t CK (MIN); IOU <sub>T</sub> = 0mA; Address and control inputs changing once per clock cycle	IDD1*	3,330	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t CK = t CK (MIN); CKE = (LOW)	IDD2P**	90	mA
IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; t CK = t CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F**	990	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t CK = t CK (MIN); CKE = LOW	IDD3P**	810	mA
ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; t RC = t RAS (MAX); t CK = t CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N**	1,080	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); IOU <sub>T</sub> = 0mA	IDD4R*	3,420	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W*	3,510	mA
AUTO REFRESH CURRENT: t RC = t RC(MIN)	IDD5*	6,210	mA
SELF REFRESH CURRENT: CKE <= 0.2V	IDD6**	90	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, t RC = t RC (MIN); t CK = t CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7*	8,100	mA
<p>* In a module with more than one rank, IDD<sub>n</sub> is calculated with one rank in IDD<sub>n</sub> and the other ranks in IDD2P.</p> <p>** All ranks in IDD<sub>n</sub>.</p> <p>where n=corresponding IDD condition listed in Symbol column.</p> <p>and Values shown for DDR SDRAM components only</p>			

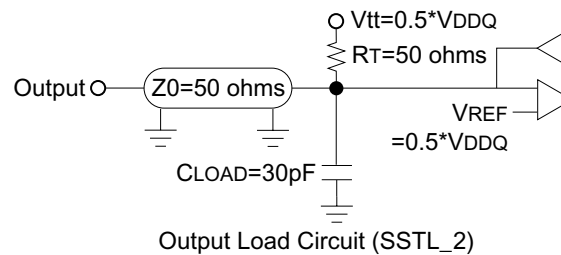
(Where U selects the RoHS Compliant, lead-free version.)

## AC OPERATING CONDITIONS

(V<sub>DD</sub>=V<sub>DDQ</sub>=2.6V, T<sub>A</sub>=0 to 70°C, f=1MHz)

Parameter/Condition	Symbol	Min	Max	Units	Note
Input High (Logic 1) Voltage, DQ, DQS, and DM signals	V <sub>IH</sub> (AC)	V <sub>REF</sub> +0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS, and DM signals	V <sub>IL</sub> (AC)		V <sub>REF</sub> -0.31	V	3
Input Differential Voltage, CK and /CK inputs	V <sub>ID</sub> (AC)	0.7	V <sub>DDQ</sub> +0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	V <sub>IX</sub> (AC)	0.5*V <sub>DDQ</sub> -0.2	0.5*V <sub>DDQ</sub> +0.2	V	2

1. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of V<sub>IX</sub> is expected to equal 0.5\*V<sub>DDQ</sub> of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relation to a V<sub>ref</sub> envelope that has been bandwidth limited 20MHz.



## CAPACITANCE

(V<sub>DD</sub>=V<sub>DDQ</sub>=2.6V, T<sub>A</sub>=25°C, f=1MHz)

Parameter	Symbol	Max	Units
Input Capacitance : A, BA, /RAS, /CAS, /WE, CKE, /S Registered Inputs. 5 pF adder for board.	C <sub>IN0</sub>	8.5	pF
Input Capacitance: CK, /CK PLL Input. 5 pF adder for board.	C <sub>IN1</sub>	8	pF
Data and DQS I/O Capacitance: DQ, CB, DQS 5 pF adder for board.	C <sub>I/O</sub>	4.5	pF

(Where U selects the RoHS Compliant, lead-free version.)

**AC TIMING PARAMETERS** (These AC characteristics were tested on the Component)

Symbol	Parameter	Min	Max	Unit	Note
tRC	Row cycle time	55		ns	
tRFC	Refresh row cycle time	70		ns	
tRAS	Row active time	40	70K	ns	
tRCD	/RAS to /CAS delay	15		ns	
tRP	Row precharge time	15		ns	
tRRD	Row active to Row active delay	10		ns	
tWR	Write recovery time	15		ns	
tWTR	Internal write to read command delay	2		tCK	
tCK	Clock cycle time	CL=3.0 CL=2.5 CL=2	5 6 7.5	12 12 12	ns
tCH	Clock high level width	0.45	0.55	tCK	4
tCL	Clock low level width	0.45	0.55	tCK	4
tDQSCK	DQS-out access time from CK, /CK	-0.60	+0.60	ns	
tAC	Output data access time from CK, /CK	CL=3.0, 2.5 CL=2	-0.70 -0.75	+0.70 +0.75	ns
tDQSQ	Data strobe edge to output data edge		0.4	ns	
tRPRE	Read Preamble	0.9	1.1	tCK	
tRPST	Read Postamble	0.4	0.6	tCK	
tDQSS	CK to valid DQS-in	0.72	1.28	tCK	
tWPRES	DQS-in setup time	0		ns	2
tWPRE	Write Preamble	0.25		tCK	
tDSS	DQS falling edge to CK rising-setup time	0.2		tCK	
tDSH	DQS falling edge from CK rising-hold time	0.2		tCK	
tDQSH	DQS-in high level width	0.35		tCK	
tDQSL	DQS-in low level width	0.35		tCK	
tIS(fast)	Address and Control Input setup time	0.6		ns	5
tIH(fast)	Address and Control Input hold time	0.6		ns	5
tIS(slow)	Address and Control Input setup time	0.7		ns	5
tIH(slow)	Address and Control Input hold time	0.7		ns	5
tHZ	Data-out high impedance time from CK,/CK	tAC max		ns	
tLZ	Data-out low impedance time from CK,/CK	tAC min		ns	
tMRD	Mode register set cycle time	10		ns	
tDS	DQ and DM setup time to DQS	0.4		ns	6,7,8
tDH	DQ and DM hold time to DQS	0.4		ns	6,7,8
tDIPW	DQ and DM input pulse width	1.75		ns	
tIPW	Control and Address input pulse width for each input	2.2		ns	
tXSNR	Exit self refresh to any Non-Read command	75		ns	
tXSRD	Exit self refresh to any Read command	200		tCK	
tREFI	Refresh interval time		7.8	μs	1
tQH	Output DQS valid window	tHPmin -tQHS		ns	
tHP	Clock half period	tCLmin or tCHmin		ns	
tQHS	Data hold skew factor		0.50	ns	
tWPST	DQS write postamble time	0.4	0.6	tCK	3
tRAP	Active to autoprecharge delay	15		ns	
N/A	Data valid output window		tQH - tDQSQ	ns	9

(Where U selects the RoHS Compliant, lead-free version.)

## Notes:

1. The refresh period is 64ms. This equates to an average refresh rate of 7.8125 $\mu$ s. However, an AUTO REFRESH command must be asserted at least once every 70.3 $\mu$ s; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High\_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. For registered DIMMs, tCL and tCH are  $\geq 45\%$  of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.

### 5. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate (V/ns)	delta tIS (ps)	delta tIH (ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t IS /t IH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

### 6. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate (V/ns)	delta tIS (ps)	delta tIH (ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t DS /t DH in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

### 7. I/O Setup/Hold Plateau Derating

I/O Input Level (mV)	delta tIS (ps)	delta tIH (ps)
$\pm 280$	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF  $\pm$  310mV for a duration of up to 2ns.

### 8. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate (ns/V)	delta tIS (ps)	delta tIH (ps)
0	0	0
$\pm 0.25$	+50	+50
$\pm 0.5$	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

9. The valid data window is derived by achieving other specifications: tHP (tCK/2), tDQSQ, and tQH (tQH = tHP - tQHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain.

## REVISION HISTORY

### Rev. Change Description from Previous Revision

- 101 10/11/2004. Initial release.
- 102 01/11/2005. Preliminary noticed removed.
- 103 01/27/2005. Currents updated to latest component dies.
- 104 03/17/2005. Title changed to VLP designation from ULP designation.
- 105 04/12/2005. Byte 47 added to SPD.
- 106 02/07/2006. Updated to latest format.
- 107 07/17/2007. Updated logo, web address and SPD.

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