

16M X 32 Bits (64MB) 144-Pin SDRAM SO-DIMM (PC100) 1 Rank x 8

## FEATURES

- PC100 Compliant  
(Option C:  $t_{CYC}=10ns@CL=3$ )  
(Option D:  $t_{CYC}=10ns@CL=2,3$ )
- Burst Mode Operation
- Auto and self refresh capability  
(4096 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V  $\pm$  0.3V power supply
- MRS cycle with address key programs
  - Latency (access from column address)
  - Burst Length (1, 2, 4, 8, and full page)
  - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- RoHS Compliant, lead-free

## GENERAL DESCRIPTION

The SL32G8E16M4G-A10xVU is a 16M x 32 bit Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM) organized in 1 rank.

The module consists of four 4M x 8 bit x 4 bank SDRAMs in 54-pin 400-mil TSOP II packages mounted in stacks of two on a 144-pin glass epoxy substrate.

A serial EEPROM using the two pin I<sup>2</sup>C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1 $\mu$ F are mounted across the power supply. Damping resistors are mounted in series on the data lines.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

See *Ordering Information* for PC100 performance options.

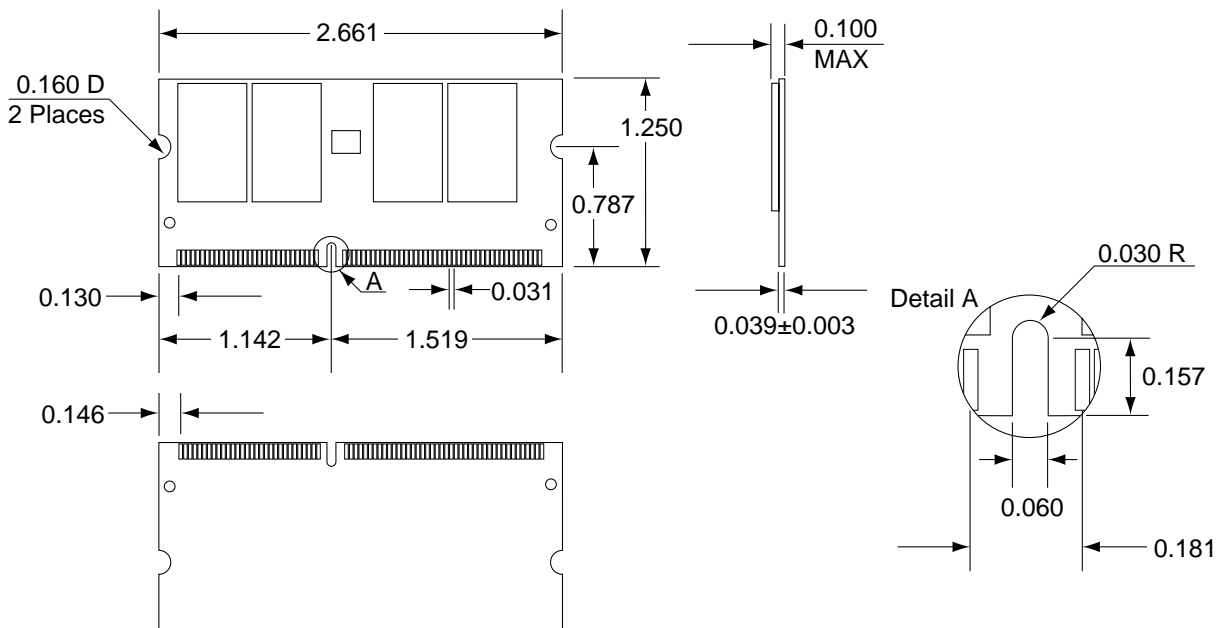
## ORDERING INFORMATION

STEC Part Number	PC100 100MHz Parameters				
	CL	t <sub>RCD</sub>	t <sub>RP</sub>	t <sub>RC</sub>	Comment
SL32G8E16M4G-A10CVU	3clks	2clks	2clks	7clks	Refer to option C in this specification
SL32G8E16M4G-A10DVU	2clks	2clks	2clks	7clks	Refer to option D in this specification

**Note:** The "U" suffix added to the part number selects the RoHS compliant lead-free version.

## PACKAGE DIMENSIONS

Units are in inches. Tolerances are  $\pm 0.005$  unless otherwise specified.



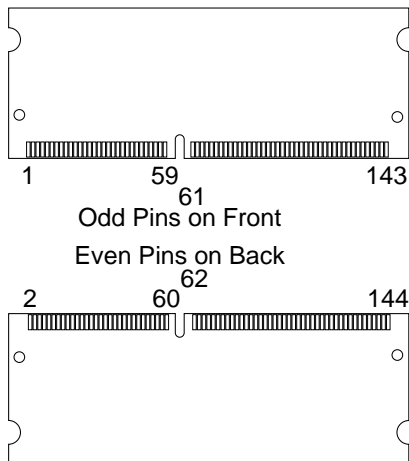
**PIN CONFIGURATION**

**Pin Symbols**

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	21	VSS	41	DQ10	61	CLK0	81	VDD	101	VDD	121	DQ24	141	SDA
2	VSS	22	VSS	42	DQ42*	62	CKE0	82	VDD	102	VDD	122	DQ56*	142	SCL
3	DQ0	23	DQMB0	43	DQ11	63	VDD	83	DQ16	103	A6	123	DQ25	143	VDD
4	DQ32*	24	DQMB4*	44	DQ43*	64	VDD	84	DQ48*	104	A7	124	DQ57*	144	VDD
5	DQ1	25	DQMB1	45	VDD	65	$\overline{RAS}$	85	DQ17	105	A8	125	DQ26		
6	DQ33*	26	DQMB5*	46	VDD	66	$\overline{CAS}$	86	DQ49*	106	BA0	126	DQ58*		
7	DQ2	27	VDD	47	DQ12	67	$\overline{WE}$	87	DQ18	107	VSS	127	DQ27		
8	DQ34*	28	VDD	48	DQ44*	68	CKE1*	88	DQ50*	108	VSS	128	DQ59*		
9	DQ3	29	A0	49	DQ13	69	$\overline{S}0$	89	DQ19	109	A9	129	VDD		
10	DQ35*	30	A3	50	DQ45*	70	A12*	90	DQ51*	110	BA1	130	VDD		
11	VDD	31	A1	51	DQ14	71	$\overline{S}1^*$	91	VSS	111	A10/AP	131	DQ28		
12	VDD	32	A4	52	DQ46*	72	A13*	92	VSS	112	A11	132	DQ60*		
13	DQ4	33	A2	53	DQ15	73	NC	93	DQ20	113	VDD	133	DQ29		
14	DQ36*	34	A5	54	DQ47*	74	CLK1*	94	DQ52*	114	VDD	134	DQ61*		
15	DQ5	35	VSS	55	VSS	75	VSS	95	DQ21	115	DQMB2	135	DQ30		
16	DQ37*	36	VSS	56	VSS	76	VSS	96	DQ53*	116	DQMB6*	136	DQ62*		
17	DQ6	37	DQ8	57	NC	77	NC	97	DQ22	117	DQMB3	137	DQ31		
18	DQ38*	38	DQ40*	58	NC	78	NC	98	DQ54*	118	DQMB7*	138	DQ63*		
19	DQ7	39	DQ9	59	NC	79	NC	99	DQ23	119	VSS	139	VSS		
20	DQ39*	40	DQ41*	60	NC	80	NC	100	DQ55*	120	VSS	140	VSS		

\* Not used

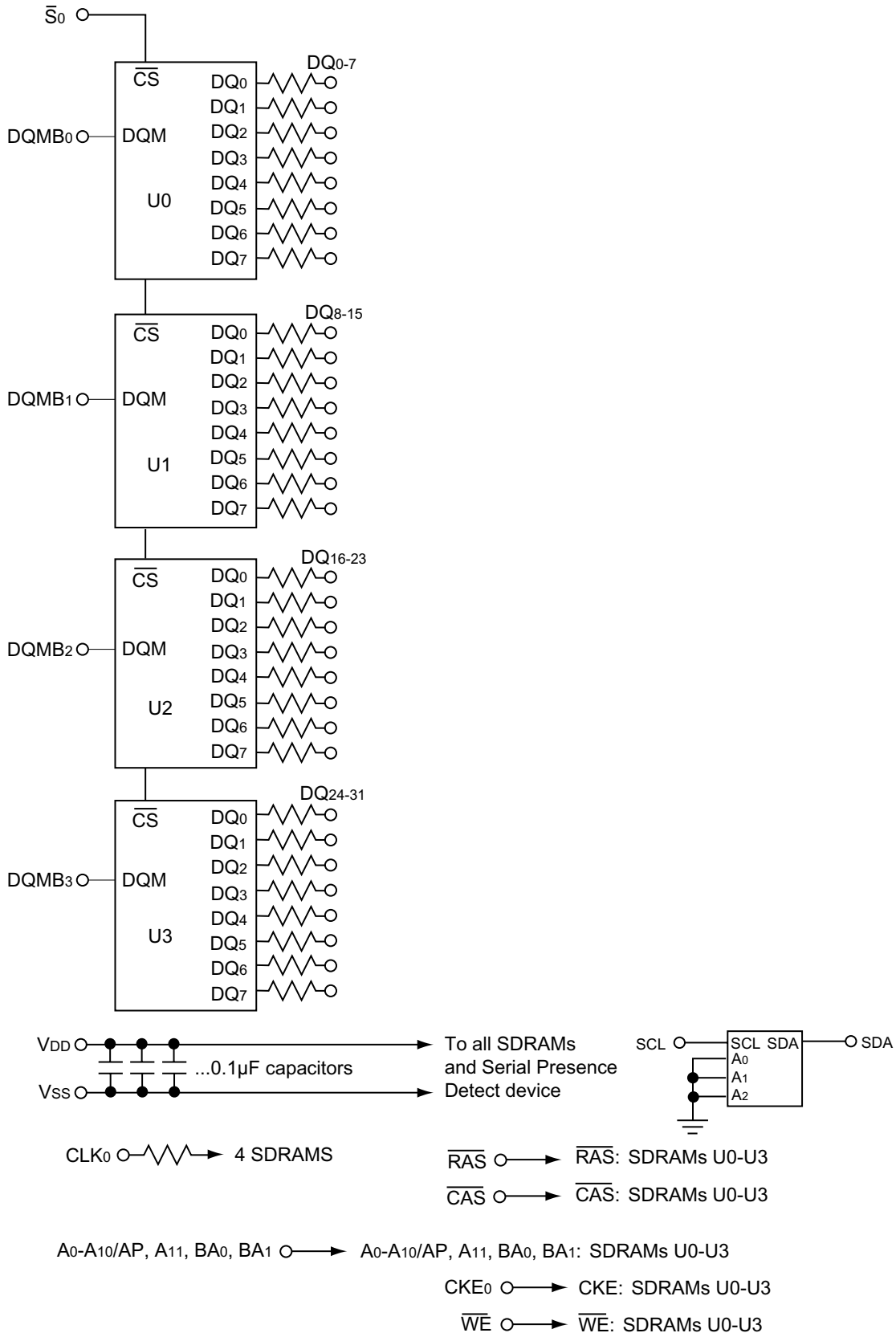
**Pin Arrangement**



**Pin Functions**

Pin Name	Pin Function
A0-A10/AP, A11	Address Inputs (multiplexed)
BA0, BA1	Select Bank
DQ0-DQ31	Data In/Out
$\overline{WE}$	Read/Write Enable
CLK0	Clock Input
CKE0	Clock Enable Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQMB0-DQMB3	Data Input/Output Mask
$\overline{S}0$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



Note: all resistors are 10 ohms.

**SERIAL PRESENCE DETECT INFORMATION**Serial PD Interface Protocol: I<sup>2</sup>C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported		Hex Value	
		Option C	Option D	Option C	Option D
0	# of bytes written into serial memory at module manufacturer	128 bytes		80h	
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)		08h	
2	Fundamental memory type	SDRAM		04h	
3	# of row addresses on this assembly	12		0Ch	
4	# of column addresses on this assembly	10		0Ah	
5	# of module ranks on this assembly	1 rank		01h	
6	Data width of this assembly	64 bits		40h	
7	...Data width of this assembly (continued)	—		00h	
8	Voltage interface standard of this assembly	LVTTL		01h	
9	SDRAM cycle time at CL=3 (t <sub>CYC</sub> )	10ns	10ns	A0h	A0h
10	SDRAM access time from clock at CL=3 (t <sub>AC</sub> )	6ns	6ns	60h	60h
11	DIMM configuration type	none		00h	
12	Refresh rate/type	15.625μs, Self-refresh		80h	
13	SDRAM width	8 bits		08h	
14	Error Checking DRAM data width	none		00h	
15	Min. CLK delay for back-to-back rand. col. addr.	t <sub>CCD</sub> =1 CLK		01h	
16	SDRAM device attributes: burst lengths supported	1,2,4,8, and full page		8Fh	
17	SDRAM device attributes: # of banks on SDRAM device	4 banks		04h	
18	SDRAM device attributes: CAS latency	CAS latency = 2,3		06h	
19	SDRAM device attributes: CS latency	CS latency = 0		01h	
20	SDRAM device attributes: Write latency	Write Latency = 0		01h	
21	SDRAM module attributes	non-buff., non-reg.		00h	
22	SDRAM device attributes: general	V <sub>CC</sub> 10%, B/R, S/W, P/A, A/P		0Eh	
23	Minimum clock cycle time at CL=2 (t <sub>CYC</sub> )	15ns	10ns	F0h	A0h
24	Max. data access time form clock at CL=2 (t <sub>AC</sub> )	8ns	6ns	80h	60h
25	Minimum clock cycle time at CL=1 (t <sub>CYC</sub> )	—	—	00h	00h
26	Max. data access time from clock at CL=1 (t <sub>AC</sub> )	—	—	00h	00h
27	Minimum row precharge time (t <sub>RP</sub> )	20ns	20ns	14h	14h
28	Minimum row active to row active delay (t <sub>RRD</sub> )	15ns	20ns	14h	14h
29	Minumum RAS to CAS (t <sub>RCD</sub> )	20ns	20ns	14h	14h
30	Minumum RAS pulse width (t <sub>RAS</sub> )	50ns	50ns	32h	32h
31	Module bank density	64MB		10h	
32	Min. command and address signal setup time (t <sub>AS</sub> )	2ns		20h	
33	Min. command and address signal hold time (t <sub>AH</sub> )	1ns		10h	
34	Min. data signal input setup time (t <sub>DS</sub> )	2ns		20h	

(Serial Presence Detect Information continued on the next page)

**SERIAL PRESENCE DETECT INFORMATION** *(continued)*

Byte #	Function Described	Function Supported		Hex Value	
		Option C	Option D	Option C	Option D
35	Min. data signal input hold time (t <sub>DH</sub> )	1ns		10h	
36-61	Superset information (may be used in future)	—		00h	
62	SPD revision	1.2		12h	
63	Checksum for bytes 0-62	JEDEC calculation		xxh	
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code		7Fh	
65	Man. JEDEC ID code (continued)	STEC's ID		A8h	
66-71				00h	
72	Manufacturing location	STEC USA or STEC Malaysia		01h (USA) or 02h	
73-90	Manufacturer's part number			xxh	
91	Revision code of PCB	RevA(01),RevB(02)		xxh	
92				00h	
93	Manufacturing date	Year (BCD)		yy	
94		Calender Week (BCD)		w w	
95	Assembly serial number	Tester number		ss	
96		Serial number (bits 7-0)		ss	
97		Serial number (bits 15-8)		ss	
98		Serial number (bits 23-16)		ss	
99-125	Manufacturer's specific data			xxh	
126	Intel specification frequency	100MHz		64h	
127	Intel specification details	Detailed 100MHz Info		8Fh	

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to VSS	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 to +4.6	V
Voltage on VCC Supply Relative to VSS	V <sub>DD</sub>	-1.0 to +4.6	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Power Dissipation	P <sub>D</sub>	4	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage reference to VSS=0, T<sub>A</sub>=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V <sub>DD</sub>	3.0	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DD</sub> +0.3	V	1
Input Low Voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output High Voltage Level	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> =-4mA
Output Low Voltage Level	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> =4mA
Input Leakage Current	I <sub>IL</sub>	-20	—	20	μA	3
Output Leakage Current	I <sub>OL</sub>	-5		5	μA	3, 4

- V<sub>IH</sub>(max)=5.6 V AC (pulse width <=3 ns acceptable).
- V<sub>IL</sub>(min) = -2.0 V AC (pulse width <=3 ns acceptable).
- Any input 0<=V<sub>IN</sub><=V<sub>DD</sub>.
- Data out is disabled, 0<=V<sub>OUT</sub><=V<sub>DD</sub>.

**CAPACITANCE** (T<sub>A</sub>=23 °C, V<sub>DD</sub>=3.3V, f=1MHz, V<sub>REF</sub>=1.4±200mA)

Item	Symbol	Max	Units
Input Capacitance (A, BA, RAS, CAS, WE) 20pF adder for board.	C <sub>IN1</sub>	40	pF
Input Capacitance (CKE, S) 20pF adder for board.	C <sub>IN2</sub>	40	pF
Input Capacitance (CLK) 10pF adder for board.	C <sub>IN3</sub>	26	pF
Input Capacitance (DQMB) 5pF adder for board.	C <sub>IN4</sub>	10	pF
Input/Output Capacitance (DQ) 5pF adder for board.	C <sub>IO1</sub>	11.5	pF

**DC CHARACTERISTICS**

Recommended operating conditions unless otherwise noted.  
 $T_A=0$  to  $70^{\circ}\text{C}$ .

Parameter/Condition	Symbol	Value (Max)	Units	Notes
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; $t_{RC} \geq t_{RC}(\text{MIN})$	IDD1	600	mA	1,3,4,5,6
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW	IDD2	8	mA	5
STANDBY CURRENT: Active Mode; CKE = HIGH; $\overline{\text{CS}}$ = HIGH; All banks active after $t_{RCD}$ met; No accesses in progress	IDD3	200	mA	1,2,4,5,6
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active	IDD4	600	mA	1,3,4,5,6
AUTO REFRESH CURRENT: $t_{RFC} = t_{RFC}(\text{MIN})$ CKE = HIGH; $\overline{\text{CS}}$ = HIGH	IDD5	1,240	mA	1,2,3,4,5,6
SELF REFRESH CURRENT: Standard CKE $\leq 0.2\text{V}$	IDD7	8	mA	

1. IDD is dependent on output loading and cycle rates.  
Specified values are obtained with minimum cycle time and the outputs open.
2. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
3. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. For Option D, CL=2 and  $t_{CK}=10\text{ns}$ . For Option A, CL=3 and  $t_{CK}=10\text{ns}$ .
6. For modules with more than one rank, IDDN is specified with one rank in IDDN and the other ranks in IDD2, where n is IDD number in the Symbol column.

## AC TIMING PARAMETERS

(AC operating conditions unless otherwise noted. Refer to the individual component, not the whole module.)

Parameter	Symbol	Min	Max	Unit	Notes
Clock Period	CL=2 CL=3	tCYC	15/10* 10	ns	
Clock High Time		tCH	3	ns	1
Clock Low Time		tCL	3	ns	
Input Setup Times		tSI	2	ns	
Input Hold Times		tHI	1	ns	
Output Valid From Clock	CL=2 CL=3	tAC		8/6* 6	2 2
Output Hold From Clock		tOH	3	ns	3
Output Valid to Z		tOHZ	3	9	ns
CAS to CAS Delay		tCCD	1	tCLK	
CAS Bank Delay		tCBD	1	tCLK	
CKE to Clock Disable		tCKE	1	tCLK	
RAS Precharge Time		tRP	2	tCLK	4
RAS Active Time		tRAS	5	tCLK	
Active to Command Delay (RAS to CAS Delay)		tRCD	2	tCLK	5
RAS to RAS Bank Activate Delay		tRRD	2	tCLK	
RAS Cycle Time		tRC	7	tCLK	6
DQM to Input Data Delay		tDQD	0	tCLK	
Write Cmd. to Input Data Delay		tDWD	0	tCLK	
Mode Register set to Active Delay		tMRD	3	tCLK	
Precharge to O/P in High-Z		tROH	CL	tCLK	
DQM to Data in HiZ for Read		tDQZ	2	tCLK	
DQM to Data Mask for Write		tDQM	0	tCLK	7
Data-In to PRE Command Period		tDPL	2	tCLK	
Data-In to ACT (PRE) Command Period (Auto Precharge)		tDAL	5	tCLK	
Power Down Mode Entry		tSB		1	tCLK
Self Refresh Exit Time		tSRX	1	tCLK	
Power Down Exit Setup Time		tPDE	1	tCLK	8
Clock Stop During Self Refresh or Power Down		tCLKSTP	200	tCLK	9

### Notes:

- Rated @ 1.5V
- LVTTL levels, rated @ 50pF, all outputs switching, 5.2ns @ 0pF
- 3ns @ 50pF, need 1.8ns @0pF
- tRP=2 a SPD Option
- tRCD=2 a SPD Option
- 7 clks for tRP=2
- Data Masked on the same clock.
- Timing is asynchronous. If tSET is not met by rising edge of CLK then CKE is assumed latched on next cycle.
- If the clock is stopped during self refresh or powerdown, 200 clocks are required before CKE is high.

## REVISION HISTORY

**Rev.** **Change Description from Previous Revision**

- 101 01/01/2001. Initial release.
- 102 06/01/2005. Component based specs updated.
- 103 07/16/2007. Logo updated. Byte 72 of SPD updated to include Malaysia.
- 104 08/24/2007. U added to part number.