

## 32M X 64 Bit (256MB) 184-Pin 1U DDR Unbuffered DIMM (PC2700) 1 Rank x 16

### FEATURES

- PC2700 Compliant  
(DDR333 166MHz-6ns; CL-tRCD-tRP=2.5-3-3 clks)
- 184-Pin UDIMM form factor
- Auto and self refresh capability  
(8192 cycles/64ms refresh)
- SSTL\_2 compatible inputs and outputs
- +2.5V  $\pm$  0.2V VDD and VDDQ
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM
- RoHS Compliant Lead Free

### GENERAL DESCRIPTION

The SL64C6M32M8L-A06EWU is a 32M x 64 bit Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Unbuffered Dual In-line Memory Module (UDIMM).

The module consists of four CMOS 8M x 16 bit x 4 bank DDR SDRAMs in 66-pin 400-mil lead-free TSOP-II packages. The DDR SDRAMs are mounted on a 184-pin glass epoxy substrate organized in 1 rank.

A serial EEPROM using the two pin IIC protocol is also mounted to provide the Serial Presence Detect (SPD) information. Decoupling capacitors are mounted in parallel across the power supply. Damping resistors are added in series on the DQ, DM, and DQS signals.

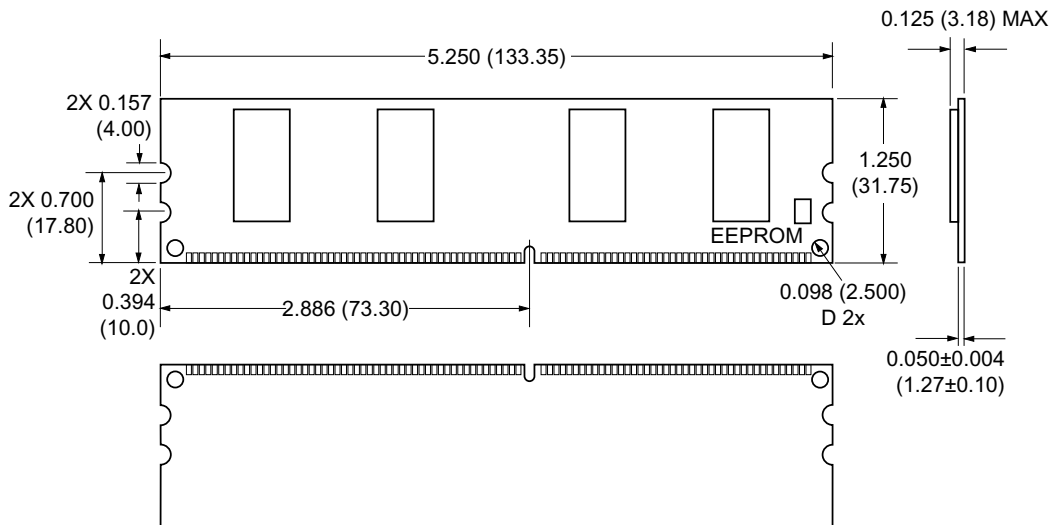
The module has gold edge connections and is intended for mounting into 184-pin UDIMM edge connector sockets keyed for 2.5V VDD and VDDQ.

### ORDERING INFORMATION

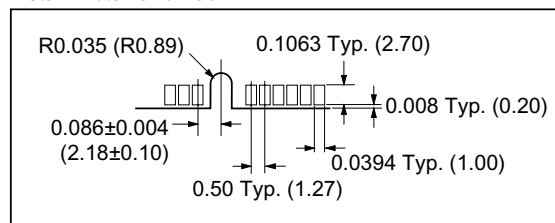
Part Number	CL	MHz	Bandwidth
SL64C6M32M8L-A06EWU	2.5	166	2.7GB/s

### PACKAGE DIMENSIONS

Units are in inches (millimeters). Tolerances are  $\pm 0.005$  ( $\pm 0.127$ ) unless otherwise specified.



Detail: Notch and Pad



## PIN CONFIGURATION (\* = Not Used; / = Active Low)

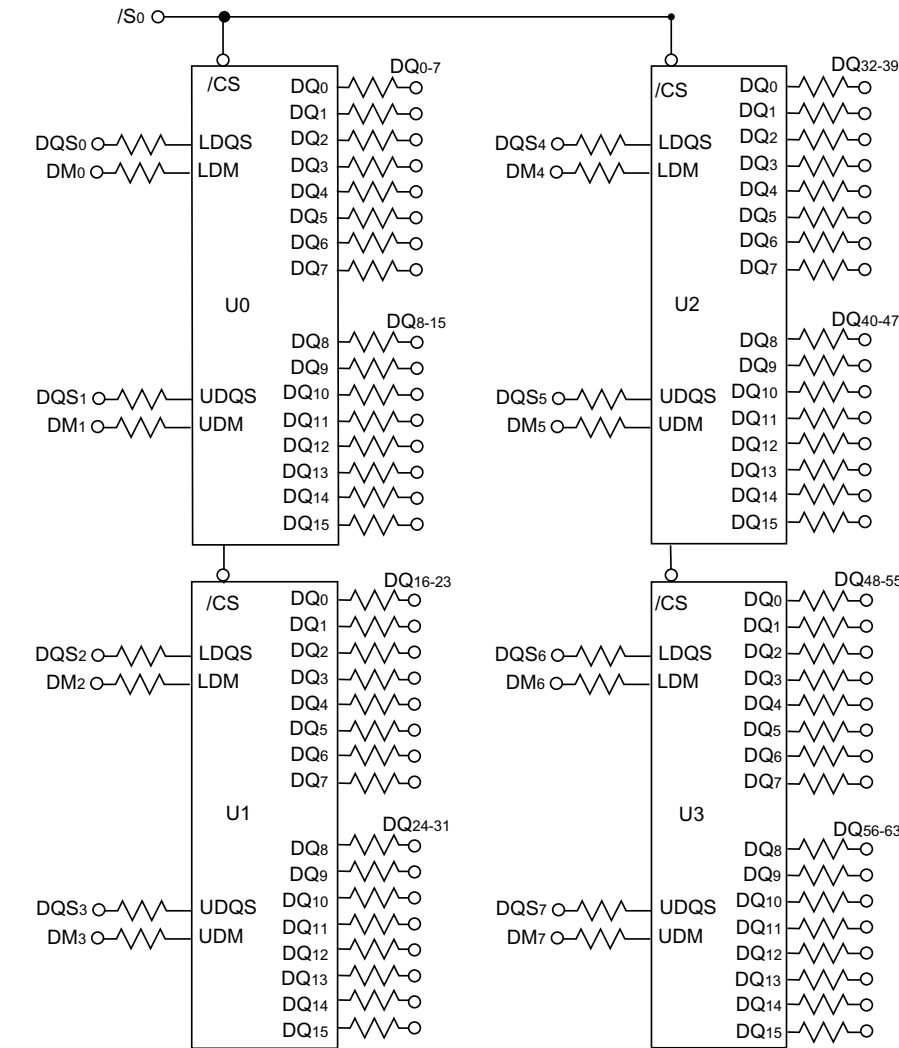
### Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	VSS	32	A5	124	VSS	62	VDDQ	154	/RAS
2	DQ0	94	DQ4	33	DQ24	125	A6	63	/WE	155	DQ45
3	VSS	95	DQ5	34	VSS	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	/CAS	157	/S0
5	DQS0	97	DM0	36	DQS3	128	VDDQ	66	VSS	158	/S1*
6	DQ2	98	DQ6	37	A4	129	DM3	67	DQS5	159	DM5
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	VSS
8	DQ3	100	VSS	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	VSS	70	VDD	162	DQ47
10	/RESET*	102	NC	41	A2	133	DQ31	71	/S2*	163	/S3*
11	VSS	103	FETEN*	42	VSS	134	CB4*	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	CB5*	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	CB0*	136	VDDQ	74	VSS	166	DQS3
14	DQS1	106	DQ13	45	CB1*	137	CK0*	75	CK2	167	A13*
15	VDDQ	107	DM1	46	VDD	138	/CK0*	76	/CK2	168	VDD
16	CK1	108	VDD	47	DQS8*	139	VSS	77	VDDQ	169	DM6
17	/CK1	109	DQ14	48	A0	140	DM8*	78	DQS6	170	DQ54
18	VSS	110	DQ15	49	CB2*	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1*	50	VSS	142	CB6*	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	CB3*	143	VDDQ	81	VSS	173	NC
21	CKE0	113	BA2*	52	BA1	144	CB7*	82	VDDID	174	DQ60
22	VDDQ	114	DQ20	Key		Key		83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	VSS	84	DQ57	176	VSS
24	DQ17	116	VSS	54	VDDQ	146	DQ36	85	VDD	177	DM7
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	VSS	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DM2	57	DQ34	149	DM4	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	VSS	150	DQ38	89	VSS	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	VDDQ	122	A8	60	DQ35	152	VSS	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

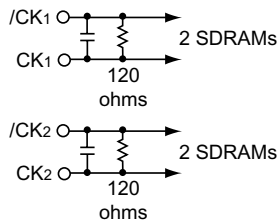
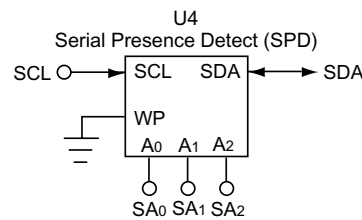
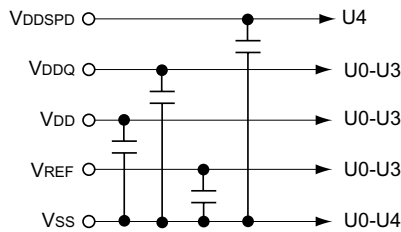
### Pin Description

Pin Symbol	Pin Description	Pin Symbol	Pin Description
A0-A11, A12, A13*	SDRAM address bus	SCL	IIC serial bus clock for EEPROM
BA0-BA1, BA2*	SDRAM bank select	SDA	IIC serial bus data line for EEPROM
DQ0-DQ63	DIMM memory data bus	SA0-SA2	IIC slave address select for EEPROM
CB0*-CB7*	DIMM ECC check bits	VDD	SDRAM positive power supply
/RAS	SDRAM row address strobe	VDDQ	SDRAM I/O driver positive power supply
/CAS	SDRAM column address strobe	VDDID	VDD Identification flag (No connect for VDD=VDDQ)
/WE	SDRAM write strobe	VREF	SDRAM I/O reference supply
/S0, /S1*, /S2*, /S3*	SDRAM chip select lines (Physical ranks 0, 1, 2, and 3)	VSS	Power supply return (ground)
CKE0, CKE1*	SDRAM clock enable lines	VDDSPD	Serial EEPROM positive power supply (2.2V to 5.5V)
DQS0-DQS7	SDRAM data strobes	NC	Spare pins (no connect)
DM0-DM7	SDRAM data mask	/RESET*	Reset pin (forces register inputs low)
CK0*, CK1, CK2	SDRAM clock (positive line of differential pair)	FETEN*	FET enable line
/CK0*, /CK1, /CK2	SDRAM clock (negative line of differential pair)		

FUNCTIONAL BLOCK DIAGRAM



- BA0-BA1 → BA0-BA1: SDRAMs U0-U3
- A0-A12 → A0-A12: SDRAMs U0-U3
- /RAS → /RAS: SDRAMs U0-U3
- /CAS → /CAS: SDRAMs U0-U3
- CKE0 → CKE0: SDRAMs U0-U3
- /WE → /WE: SDRAMs U0-U3



- NOTES:
1. DQ wiring may be changed within a byte.
  2. DQ, DQS, DM, CKE, /S relationships must be maintained as shown.
  3. DQ, DQS, and DM resistors are 22 ohms.

## SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: IIC; Current sink capability of SDA driver  $\leq 3\text{mA}$ ; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128	80h
1	Total # of bytes of SPD memory device	256	08h
2	Fundamental memory type	DDR SDRAM	07h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	10	0Ah
5	# of physical ranks on this assembly	1 rank	01h
6	Data width of this assembly	64 bits	40h
7	Data width of this assembly (continued)	—	00h
8	Voltage interface level of this assembly	SSTL 2.5V	04h
9	SDRAM cycle time at CL=2.5 (tCYC)	6ns	60h
10	SDRAM access time from clock at CL=3 (tAC)	0.7ns	70h
11	DIMM configuration type	None	00h
12	Refresh rate/type	7.8 $\mu\text{s}$ , Self -refresh	82h
13	SDRAM width	16 bits	10h
14	Error Checking SDRAM data width	None	00h
15	Min. CLK delay for back-to-back rand. col. addr.	tCCD=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	2,4,8	0Eh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5	0Ch
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 1	02h
21	SDRAM module attributes	Differential Clock	20h
22	SDRAM device attributes: general	Fast/Concurrent AP, Weak Driver	C1h
23	Minimum clock cycle time at CL=2 (tCYC)	7.5ns	75h
24	Max. data access time from clock at CL=2.5 (tAC)	0.7ns	70h
25	Minimum clock cycle time at CL=1.5 (tCYC)	--	00h
26	Max. data access time from clock at CL=1.5 (tAC)	--	00h
27	Minimum row precharge time (tRP)	18ns	48h
28	Minimum row active to row active delay (tRRD)	12ns	30h
29	Minumum RAS to CAS (tRCD)	18ns	48h
30	Minumum RAS pulse width (tRAS)	42ns	2Ah
31	Module bank density	256MB	40h
32	Min. command and address signal setup time (tIS)	0.75ns	75h
33	Min. command and address signal hold time (tIH)	0.75ns	75h
34	Min. data/data mask signal input setup time (tDS)	0.45ns	45h
35	Min. data/data mask signal input hold time (tDH)	0.45ns	45h

(Serial Presence Detect continued on the next page)

**SERIAL PRESENCE DETECT INFORMATION** (continued)

Byte #	Function Described	Function Supported	Hex Value
36-40	Reserved		00h
41	Row cycle time (tRC)	60ns	3Ch
42	Auto refresh cycle time (tRFC)	72ns	45h
43	Maximum SDRAM device cycle time (tCK_MAX)	12ns	30h
44	DQS-DQ skew (tDQSQ)	0.45ns	2Dh
45	SDRAM device data hold skew factor (tQHS)	0.55ns	55h
46	Reserved		00h
47	DDR SDRAM DIMM height	1.125" to 1.25" (1.25")	01h
48-61	Reserved		00h
62	SPD revision	JEDEC initial release	00h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71			00h
72	Manufacturing location	STEC USA	xxh
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	RevA(01),RevB(02)	xxh
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	ww
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-127	Manufacturer's specific data		xxh
128-255	Open for Customer Use	Undefined	00h

## ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional Operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time may affect device reliability.

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	VIN, VOUT	-1.0 to +3.6	V
Voltage on VDD supply relative to VSS	VDD	-1.0 to +3.6	V
Voltage on VDDQ supply relative to VSS	VDDQ	-1.0 to 3.6	V
Storage temperature	TSTG	-55 to +150	°C
Power Dissipation	PD	6	W
Short circuit current	IOS	50	mA

## POWER and DC OPERATING CONDITIONS (SSTL\_2 IN/OUT)

Recommended operating conditions (Voltage referenced to VSS=0V.)

Parameter	Symbol	Min	Max	Unit	Notes
Operating Temperature	TA	0	70	°C	
Supply Voltage (for device with a nominal VDD of 2.6V)	VDD	2.3	2.7	V	
I/O Supply voltage	VDDQ	2.3	2.7	V	
I/O Reference voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	1
I/O Termination voltage (system)	VTT	VREF-0.04	VREF+0.04	V	2
Input logic high voltage	VIH(DC)	VREF+0.15	VDDQ+0.3	V	4
Input logic low voltage	VIL(DC)	-0.3	VREF-0.15	V	4
Input voltage level, CK and /CK	VIN(DC)	-0.3	VDDQ+0.3	V	
Input differential voltage, CK and /CK	VID(DC)	0.36	VDDQ+0.6	V	3
Input leakage current	A, BA, /RAS, /CAS, /WE CKE, /S CK1-2, /CK1-2 DM	-8 -8 -4 -2	8 8 4 2	μA μA μA μA	
Output leakage current	DQ, DQS	IOZ	-5	5	μA
Output high current (VOUT= VDDQ - 0.373V, minimum VREF, minimum VT)	IOH	-16.8			mA
Output low current (VOUT= 0.373V, maximum VREF, maximum VTT)	IOL	16.8			mA

1. Includes  $\pm 25\text{mV}$  margin for DC offset on VREF, and a combined total of  $\pm 50\text{mV}$  margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in V REF noise. VREF should be de-coupled with an inductance of  $\leq 3\text{nH}$ .
2. V TT is not applied directly to the device. V TT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
5. The value of VIX is expected to equal  $0.5*VDDQ$  of the transmitting device and must track variations in the dc level of the same.
6. These characteristics obey the SSTL-2 class II standards.

## DC CHARACTERISTICS

### Maximum DDR IDD Values

- For IDD0, IDD1, IDD4R, IDD4W, IDD5, and IDD7:  
In a module with more than one rank, IDDn is calculated with one rank in the IDDn and the other ranks in IDD2P.  
For IDD2P, IDD2F, IDD3P, IDD3N, and IDD6:  
All ranks in IDDn.  
where n=corresponding IDD condition listed in Symbol column.
- Values shown for DDR2 SDRAM components only.
- Values will differ depending on DRAM parts used on the module.
- IDD values are calculated using worst case specifications of currently available DRAMs from different manufacturers.

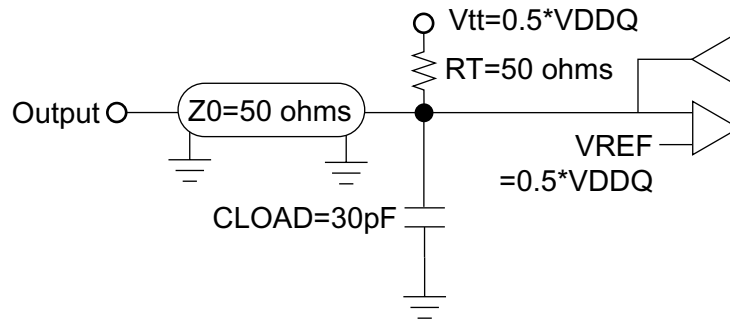
Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; t RC = t RC (MIN); t CK = t CK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;	IDD0	620	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; t RC = t RC (MIN); t CK = t CK (MIN); IOU = 0mA; Address and control inputs changing once per clock cycle	IDD1	780	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t CK = t CK (MIN); CKE = (LOW)	IDD2P	20	mA
IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; t CK = t CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	220	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t CK = t CK (MIN); CKE = LOW	IDD3P	180	mA
ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; t RC = t RAS (MAX); t CK = t CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	240	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); IOU = 0mA	IDD4R	860	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	860	mA
AUTO REFRESH CURRENT: t RC = t RC(MIN)	IDD5	1,380	mA
SELF REFRESH CURRENT: CKE <= 0.2V	IDD6	24	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) withauto precharge, t RC = t RC (MIN); t CK = t CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7	1,920	mA

## AC OPERATING CONDITIONS

(VDD=VDDQ=2.5V, TA=0 to 70°C, f=1MHz)

Parameter/Condition	Symbol	Min	Max	Units	Note
Input High (Logic 1) Voltage, DQ, DQS, and DM signals	V <sub>IH</sub> (AC)	V <sub>REF</sub> +0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS, and DM signals	V <sub>IL</sub> (AC)		V <sub>REF</sub> -0.31	V	3
Input Differential Voltage, CK and /CK inputs	V <sub>ID</sub> (AC)	0.7	V <sub>DDQ</sub> +0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	V <sub>IX</sub> (AC)	0.5*V <sub>DDQ</sub> -0.2	0.5*V <sub>DDQ</sub> +0.2	V	2

1. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of V<sub>IX</sub> is expected to equal 0.5\*V<sub>DDQ</sub> of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relation to a V<sub>ref</sub> envelope that has been bandwidth limited 20MHz.



Output Load Circuit (SSTL\_2)

## CAPACITANCE

(VDD=VDDQ=2.5V, TA=25°C, f=1MHz)

Parameter	Symbol	Max	Units
Input Capacitance : A, BA, /RAS, /CAS, /WE, CKE, /S 30 pF added for board.	CIN0	42	pF
Input Capacitance: CK1-2, /CK1-2 15 pF added for board.	CIN1	21	pF
Data and DQS I/O and DM Input capacitance: DQ, DQS, DM 5 pF added for board.	CI/O	10	pF

**AC TIMING PARAMETERS** (These AC characteristics were tested on the component)

Symbol	Parameter	Min	Max	Unit	Note
tRC	Row cycle time	60		ns	
tRFC	Refresh row cycle time	72		ns	
tRAS	Row active time	42	70K	ns	
tRCD	/RAS to /CAS delay	18		ns	
tRP	Row precharge time	18		ns	
tRRD	Row active to Row active delay	15		ns	
tWR	Write recovery time	15		ns	
tWTR	Internal write to read command delay	1		tCK	
tCK	Clock cycle time	CL=2.0 CL=2.5	7.5 6 12 12		
tCH	Clock high level width	0.45	0.55	tCK	4
tCL	Clock low level width	0.45	0.55	tCK	4
tDQSCK	DQS-out access time from CK, /CK	-0.60	+0.6	ns	
tAC	Output data access time from CK, /CK	-0.70	+0.7	ns	
tDQSQ	Data strobe edge to output data edge		+0.45	ns	
tRPRE	Read Preamble	0.9	1.1	tCK	
tRPST	Read Postamble	0.4	0.6	tCK	
tDQSS	CK to valid DQS-in	0.75	1.25	tCK	
tWPRES	DQS-in setup time	0		ns	2
tWPRE	Write Preamble	0.25		tCK	
tDSS	DQS falling edge to CK rising-setup time	0.2		tCK	
tDSH	DQS falling edge from CK rising-hold time	0.2		tCK	
tDQSH	DQS-in high level width	0.35		tCK	
tDQSL	DQS-in low level width	0.35		tCK	
tIS(fast)	Address and Control Input setup time	0.75		ns	5
tIH(fast)	Address and Control Input hold time	0.75		ns	5
tIS(slow)	Address and Control Input setup time	0.8		ns	5
tIH(slow)	Address and Control Input hold time	0.8		ns	5
tHZ	Data-out high impedance time from CK,/CK	-0.7	0.7	ns	
tLZ	Data-out low impedance time from CK,/CK	-0.7	0.7	ns	
tMRD	Mode register set cycle time	2		tCK	
tDS	DQ and DM setup time to DQS	0.45		ns	6,7,8
tDH	DQ and DM hold time to DQS	0.45		ns	6,7,8
tDIPW	DQ and DM input pulse width	1.75		ns	
tIPW	Control and Address input pulse width for each input	2.2		ns	
tXSNR	Exit self refresh to any Non-Read command	75		ns	
tXSRD	Exit self refresh to any Read command	200		tCK	
tREFI	Refresh interval time		7.8	μs	1
tQH	Output DQS valid window	tHPmin -tQHS		ns	
tHP	Clock half period	tCLmin or tCHmin		ns	
tQHS	Data hold skew factor		0.5	ns	
tWPST	DQS write postamble time	0.4	0.6	tCK	3
tRAP	Active to autoprecharge delay	18		ns	
N/A	Data valid output window		tQH - tDQSQ	ns	9

**Notes:**

1. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High\_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. For registered DIMMs, tCL and tCH are >= 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.

5. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	delta tIS	delta tIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t IS /t IH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

6. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	delta tDS	delta tDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t DS /t DH in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Plateau Derating

I/O Input Level	delta tDS	delta tDH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

8. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	delta tDS	delta tDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

9. The valid data window is derived by achieving other specifications: tHP (tCK/2), tDQSQ, and tQH (tQH = tHP - tQHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain.

**REVISION HISTORY**

**Rev. Change Description from Previous Revision**

- 101 09/01/2006. Initial release.
- 102 07/24/2007. Updated logo, web address and SPD.