

32M x 64 Bit (256MB) 144-Pin SDRAM SO-DIMM (PC133) 1 Rank x 8; RoHS Compliant, Lead-Free

FEATURES

- PC133 Compliant
(Option A: tCYC = 7.5ns@CL = 3)
(Option B: tCYC = 7.5ns@CL = 2, 3)
- 144-Pin SO-DIMM form factor
- Burst Mode Operation
- Auto and Self Refresh capability
(8,192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V +/-0.3V power supply
- MRS cycle with address key programs
-Latency (access from column address)
-Burst Length (1, 2, 4, 8 and Full Page)
-Data Scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts
- RoHS Compliant, lead-free

GENERAL DESCRIPTION

The SL64G8F32M8G-C75xVU is a 32M x 64 bit (256MB) 144-pin Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of eight 8M x 8 bit x 4 bank SDRAMs in lead-free 54-pin 400-mil TSOP II packages mounted in 1 rank on a 144-pin glass epoxy substrate.

A serial EEPROM using the two pin I²C protocol is also mounted to provide the Serial Presence Detects (SPD). Decoupling capacitors of 0.1µF are mounted.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

Notes:

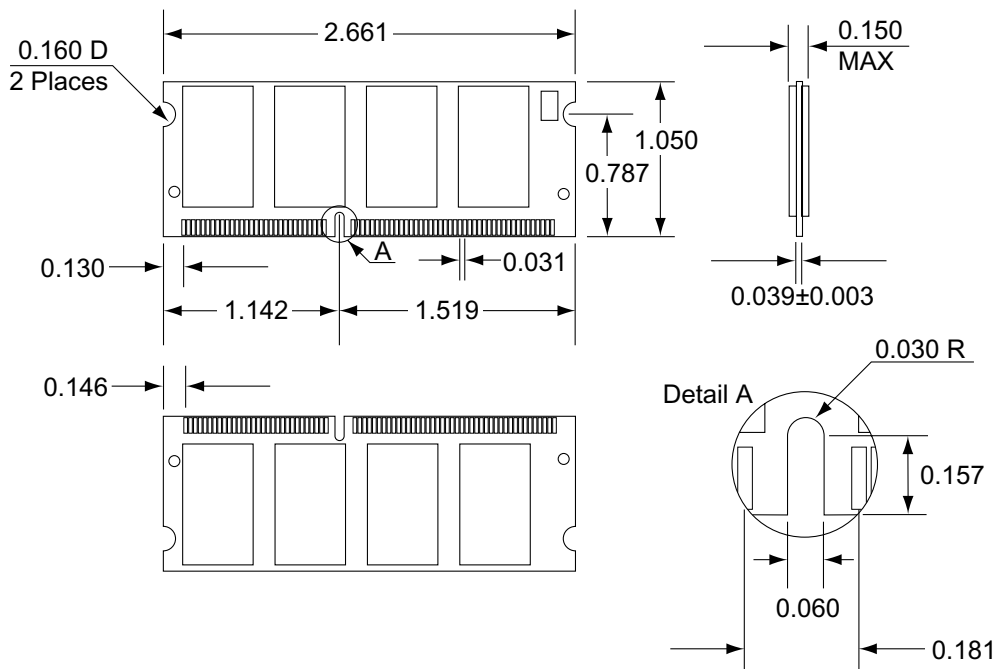
1. No damping resistors are used on the data lines.
2. See the Ordering Information table for PC133 performance options.

ORDERING INFORMATION

Part Number	PC133 133MHz Parameters				Comment
	CL	tRCD	tRP	tRC	
SL64G8F32M8G-C75AVU	3clks	20ns	20ns	66ns	Refer to Option A in this specification.
SL64G8F32M8G-C75DVU	2clks	15ns	15ns	60ns	Refer to Option B in this specification.

PACKAGE DIMENSIONS (Board No.: 596)

Units are in inches. All dimensions are typical unless otherwise specified.

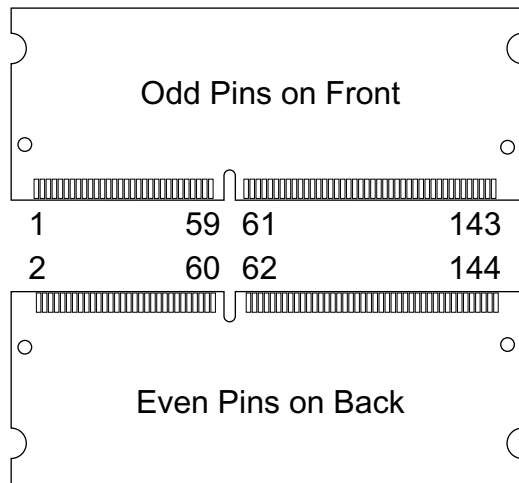


PIN CONFIGURATION

144-PIN SO-DIMM PINOUT

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	21	VSS	41	DQ10	61	CLK0	81	VDD	101	VDD	121	DQ24	141	SDA
2	VSS	22	VSS	42	DQ42	62	CKE0	82	VDD	102	VDD	122	DQ56	142	SCL
3	DQ0	23	DQMB0	43	DQ11	63	VDD	83	DQ16	103	A6	123	DQ25	143	VDD
4	DQ32	24	DQMB4	44	DQ43	64	VDD	84	DQ48	104	A7	124	DQ57	144	VDD
5	DQ1	25	DQMB1	45	VDD	65	/RAS	85	DQ17	105	A8	125	DQ26		
6	DQ33	26	DQMB5	46	VDD	66	/CAS	86	DQ49	106	BA0	126	DQ58		
7	DQ2	27	VDD	47	DQ12	67	/WE	87	DQ18	107	VSS	127	DQ27		
8	DQ34	28	VDD	48	DQ44	68	CKE1*	88	DQ50	108	VSS	128	DQ59		
9	DQ3	29	A0	49	DQ13	69	S0	89	DQ19	109	A9	129	VDD		
10	DQ35	30	A3	50	DQ45	70	A12	90	DQ51	110	BA1	130	VDD		
11	VDD	31	A1	51	DQ14	71	/S1*	91	VSS	111	A10/AP	131	DQ28		
12	VDD	32	A4	52	DQ46	72	A13*	92	VSS	112	A11	132	DQ60		
13	DQ4	33	A2	53	DQ15	73	NC	93	DQ20	113	VDD	133	DQ29		
14	DQ36	34	A5	54	DQ47	74	CLK1	94	DQ52	114	VDD	134	DQ61		
15	DQ5	35	VSS	55	VSS	75	VSS	95	DQ21	115	DQMB2	135	DQ30		
16	DQ37	36	VSS	56	VSS	76	VSS	96	DQ53	116	DQMB6	136	DQ62		
17	DQ6	37	DQ8	57	CB0*	77	CB2*	97	DQ22	117	DQMB3	137	DQ31		
18	DQ38	38	DQ40	58	CB4*	78	CB6*	98	DQ54	118	DQMB7	138	DQ63		
19	DQ7	39	DQ9	59	CB1*	79	CB3*	99	DQ23	119	VSS	139	VSS		
20	DQ39	40	DQ41	60	CB5*	80	CB7*	100	DQ55	120	VSS	140	VSS		

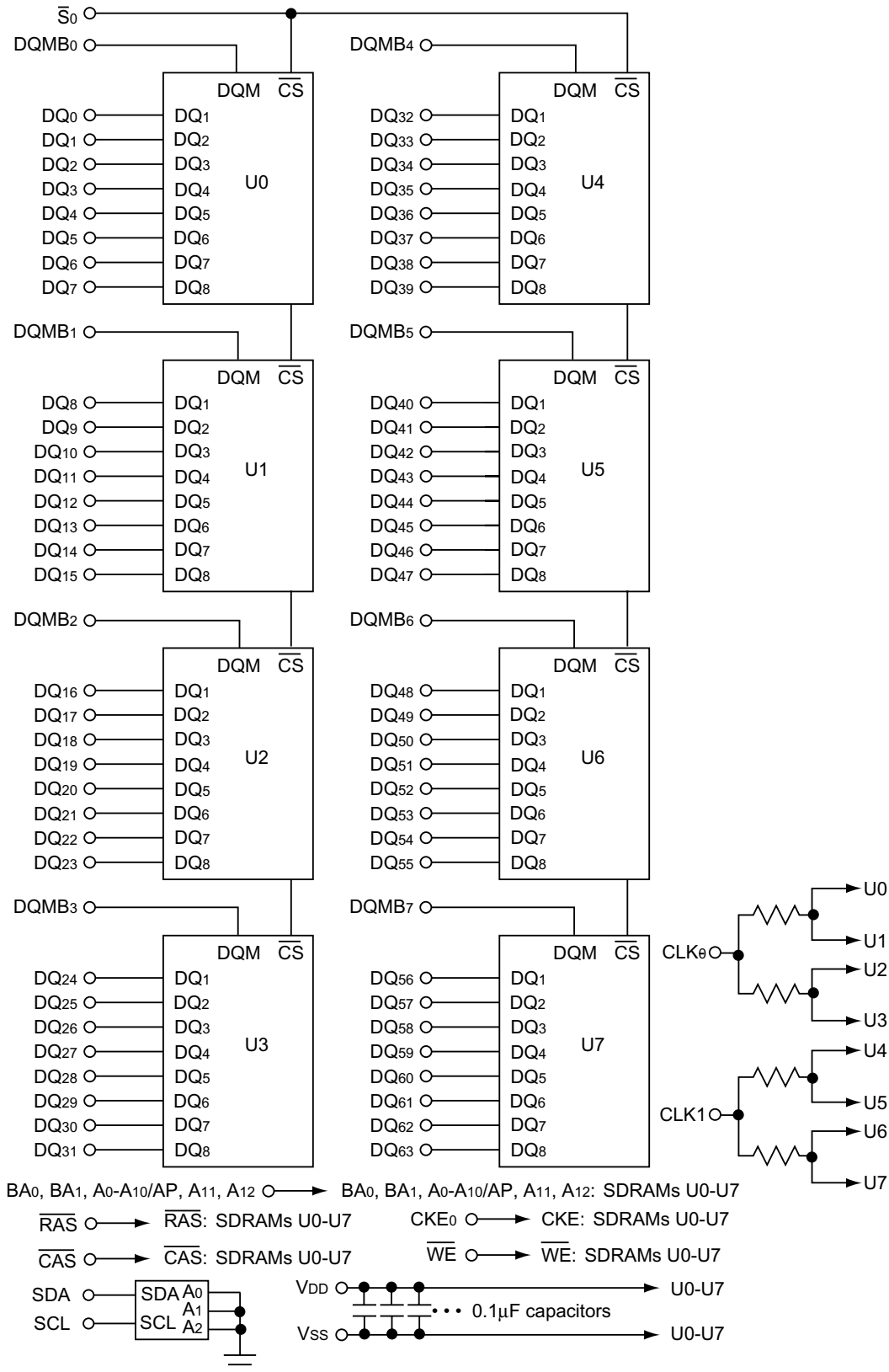
PIN LOCATIONS



PIN FUNCTIONS

Pin Symbol	Pin Function
A0-A10/AP, A11, A12	Address Inputs (Multiplexed)
BA0, BA1	Select Bank
DQ0-DQ63	Data In/Out
/WE	Read/Write Enable
CLK0, CLK1	Clock Input
CKE0	Clock Enable Input
/RAS	Row Address Strobe
/CAS	Column Address Strobe
DQMB0-DQMB7	Data Input/Output Mask
/S0	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I2C; Current sink capability of SDA driver $\leq 3\text{mA}$; Maximum Clock Frequency: 100KHz

Byte	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
0	Number of Bytes Written into Serial Memory	128		80h	
1	Total Number of Bytes of SPD Device	256 (2K-bit)		08h	
2	Fundamental Memory Type	SDRAM		04h	
3	Number of Row Addresses on Assembly	13		0Dh	
4	Number of Column Addresses on Assembly	10		0Ah	
5	Number of Module Banks on Assembly	1		01h	
6	Data Width of Assembly	64		40h	
7	Reserved	-		00h	
8	Voltage Interface Level	LVTTTL		01h	
9	SDRAM Cycle Time at CL = 3, tCYC	7.5ns	7.5ns	75h	75h
10	SDRAM Access Time from Clock at CL = 3, tAC	5.4ns	5.4ns	54h	54h
11	DIMM Configuration Type	None		00h	
12	Refresh Rate/Type	7.8 μ s/SELF		82h	
13	SDRAM Width	x8		08h	
14	Error Checking DRAM Data Width	None		00h	
15	Min. CLK Delay for Back-to-Back Rand. Col. Addr.	tCCD = 1 CLK		01h	
16	SDRAM Device Attributes: Burst Lengths Supported	1, 2, 4, 8/Full Page		8Fh	
17	SDRAM Device Attributes: No. of Banks on SDRAM Device	4		04h	
18	SDRAM Device Attributes: CAS Latency	2, 3		06h	
19	SDRAM Device Attributes: CS Latency	0		01h	
20	SDRAM Device Attributes: Write Latency	0		01h	
21	SDRAM Module Attributes	None		00h	
22	SDRAM Device Attributes: General	VCC 10%, B/R, S/W P/A, A/P		0Eh	
23	Minimum Clock Cycle Time at CL = 2, tCYC	10ns	75ns	A0h	75h
24	Maximum Data Access Time from Clock at CL = 2, tAC	6ns	5.4ns	60h	54h
25	Minimum Clock Cycle Time at CL = 1, tCYC	-	-	00h	00h
26	Maximum Data Access Time from Clock at CL = 1, tAC	-	-	00h	00h
27	Minimum Row Precharge Time, tRP	20ns	15ns	14h	0Fh
28	Minimum Row Active to Row Active Delay, tRRD	15ns	15ns	0Fh	0Fh
29	Minimum /RAS to /CAS, tRCD	20ns	15ns	14h	0Fh
30	Minimum /RAS Pulse Width, tRAS	45ns	45ns	2Dh	2Dh
31	Module Rank Density	256MB		40h	
32	Minimum Command and Address Signal Setup Time, tAS	1.5ns		15h	
33	Minimum Command and Address Signal Hold Time, tAH	0.8ns		08h	
34	Minimum Data Signal Input Setup Time, tDS	1.5ns		15h	

(Serial Presence Detect Information continued on next page.)

SERIAL PRESENCE DETECT INFORMATION *(continued)*Serial PD Interface Protocol: I2C; Current sink capability of SDA driver $\leq 3\text{mA}$; Maximum Clock Frequency: 100KHz

Byte	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
35	Minimum Data Signal Input Hold Time, tDH	0.8ns		08h	
36 - 61	Superset Information (Reserved for Future Use)	-		00h	
62	SPD Revision	1.2		12h	
63	Checksum for Bytes 0 - 62	JEDEC Calculation		xxh	
64	Manufacturer's JEDEC ID Code per JEP-106E	Continuation Code		7Fh	
65	Manufacturer's JEDEC ID Code (Continued)	STEC's ID		A8h	
66 - 71	-	-		00h	
72	Manufacturing Location STEC USA (01h) STEC Malaysia (02h)	USA (01h) or Malaysia (02h)		01h 02h	
73 - 90	Manufacturer's Part Number			xxh	
91	PCB Revision Code	Eng (00) Rev A (01) Rev B (02)		01h	
92				00h	
93	Manufacturing Date	Year (BCD)		yyh	
94		Week (BCD)		wwh	
95	Assembly Serial Number	Tester Number		ssh	
96		Serial Number (Bits 7-0)		ssh	
97		Serial Number (Bits 15-8)		ssh	
98		Serial Number (Bits 23-16)		ssh	
99 - 125	Manufacturer's Specific Data			xxh	
126	Intel Specification Frequency	100MHz		64h	
127	Intel Specification Details	Detailed 100MHz Info		CFh	

ABSOLUTE MAXIMUM DC RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to higher than recommended voltages for extended periods may affect device reliability.

Symbol	Parameter	Rating	Units
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to +4.6	V
VDD	Voltage on VCC Supply Relative to VSS	-1.0 to +4.6	V
Tstg	Storage Temperature	-55 to +150	°C
PD	Power Dissipation	8	W
IOS	Short Circuit Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

(Voltage referenced to VSS = 0, TA = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD	Supply Voltage	3	3.3	3.6	V	
VIH	Input High Voltage	2	3	VDD+0.3	V	1
VIL	Input Low Voltage	-0.3	0	0.8	V	2
VOH	Output High Voltage Level	2.4	—	—	V	IOH=-2mA
VOL	Output Low Voltage Level	—	—	0.4	V	IOL=2mA
IIL	Input Leakage Current	-80	—	80	µA	3

Notes:

1. VIH(max)=5.6 V AC (pulse width ≤ 3 ns acceptable)
2. VIL(min) = -2.0 V AC (pulse width ≤ 3 ns acceptable)
3. Any input $0 \leq V_{IN} \leq V_{DD}$. Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(TA = 23°C, VDD = 3.3V, f = 1MHz, VREF = 1.4 +/-200mA)

Symbol	Parameter	Max	Units
CIN1	Input Capacitance (A0-A10/AP, A11, A12, BA0, BA1)	41	pF
CIN2	Input Capacitance (/RAS, /CAS, /WE)	41	pF
CIN3	Input Capacitance (CLK0)	19	pF
CIN4	Input Capacitance (CKE0)	41	pF
CIN5	Input Capacitance (/S0)	41	pF
CIN6	Input Capacitance (DQMB0-DQMB7)	14	pF
CIO1	Input/Output Capacitance (DQ0-DQ63)	16	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted. TA = 0 to 70°C.)

Symbol	Parameter	Test Condition		Max	Units
ICC1S	Operating Current (One Bank Active)	Burst length=1, tRC>=tRC(min), IOL=0mA, Outputs open	Option A	880	mA
			Option D	960	mA
ICC2P	Precharge Standby Current in Power-Down Mode	CKE<=VIL(max), tCLK=10ns, CKE and CLK<=VIL(max), tCLK=∞		16	mA
ICC2PS				16	mA
ICC2N	Precharge Standby Current in Non Power-Down Mode	CKE and S.>=VIH(min), tCLK=10ns Input signals are changed one time during 20ns. CKE>=VIH(min), CLK<= VIL(max), tCLK=∞ Input signals are stable		160	mA
ICC2NS				80	mA
ICC3P	Active Standby Current in Power-Down Mode	CKE>= VIL(max), tCLK=10ns CKE and CLK<=VIL(max), tCLK=∞		48	mA
ICC3PS				48	mA
ICC3N	Active Standby Current in Non Power-Down Mode (One Bank Active)	CKE and S.>=VIH(min), tCLK=10ns, Input signals are changed one time during 20ns. CKE>=VIH(min), CLK<=VIL(max), tCLK=∞ Inputs are stable		270	mA
ICC3NS				200	mA
ICC4	Operating Current (Burst Mode)	IOL=0mA, Page Burst, 4 banks activated ICCD=2 CLKs, Outputs open		1040	mA
ICC5	Refresh Current (Refresh Period is 64ms)	tRC>=tRC(min)	Option A	1600	mA
			Option D	1760	mA
ICC6	Self Refresh Current	CKE<=0.2V		24	mA

AC TIMING PARAMETERS (TA = 0 TO 65oC; VCC = 3.0V - 3.6V; CL = 2, 3)

		Speed Grade		Speed Grade		Unit		Notes	
		100MHz		133MHz/100MHz					
Symbol	Parameter	Min	Max	Min	Max				
tCLK	Clock Period	10		7.5		ns			
tCH	Clock High Time (Rated @ 1.5V)	3		2.5		ns			
tCL	Clock Low Time	3		2.5		ns			
tSI	Input Setup Times:								
	(Data)	2		1.5		ns			
tHI	Input Hold Times:								
	(Data)	1		0.8		ns			
tAC	Output Valid from Clock		7.0		N/A	ns		1	
	(CL = 2; limited application; 2 banks; all outputs switching)								
tAC	Output Valid from Clock (CL = 2; LVTTTL levels; Rated @ 50pF; all outputs switching)		6.0 (tCO = 5.2)		5.4 (tCO = 4.6)	ns		1	
tAC	Output Valid from Clock (CL = 3; LVTTTL levels; Rated @ 50pF; all outputs switching)		6.0 (tCO = 5.2)		5.4 (tCO = 4.6)	ns		1	
tOH	Output Hold from Clock (Rated @ 50pF; 1.8ns@0pF)	3		2.7		ns			
tOHZ	Output Valid to Z	3	9	2.7	7	ns			
tCCD	CAS to CAS Delay	1		1		tCLK			
tCBD	CAS Bank Delay	1		1		tCLK			
tCKE	CKE to Clock Disable	1		1		tCLK			
tRP	RAS Precharge Time								
	Option D	15.0		15.0		ns			
tRAS	RAS Active Time	50		45		ns			
	Option A	20.0		20.0		ns			
rRCD	Active to Command Delay (RAS to CAS Delay)								
	Option D	15.0		15.0		ns			
tRRD	RAS to RAS Bank Activate Delay	20		15		ns			
	Option A	20.0		20.0		ns			
tRC	RAS Cycle Time								
	Option D	N/A		60		ns			
tDQD	DQM to Input Data Delay	0		0		tCLK			
	Option A	70		66		ns			

(AC Timing Parameters continued on next page.)

AC TIMING PARAMETERS (Continued)

		Speed Grade		Speed Grade			
		100MHz		133MHz/100MHz			
Symbol	Parameter	Min	Max	Min	Max	Unit	Notes
tDWD	Write Command to Input Data Delay	0		0		tCLK	
tMRD	Mode Register Set to Active Delay	3		3		tCLK	
tROH	Precharge to O/P in High-Z		CL		CL	tCLK	2
tDQZ	DQM to Data in Hi-Z for Read	2		2		tCLK	
tDQM	DQM to Data Mask for Write	0		0		tCLK	3
tDPL	Data-In to PRE-Command Period	20		15		ns	
tDAL	Data-In to ACT (PRE) Command Period (Auto Precharge)	5		5		tCLK	
tSB	Power Down Mode Entry		1		1	tCLK	
tSRX	Self-Refresh Exit Time	10		10		ns	4
tPDE	Power Down Exit Setup Time	1		1		tCLK	5
tCLKSTP	Clock Stop during Self-Refresh or Power Down	200		200		tCLK	6
tREF	Refresh Period		64		64	ms	7
tRFC	Row Refresh Cycle Time	80.0		75.0		ns	

Notes:

1. Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V. t_{ACN}=access time with 0pF load.
2. CL = CAS Latency.
3. Data Masked on the same clock.
4. Self-Refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + t_{RC}.
5. Timing is asynchronous. If t_{set} is not met by rising edge of CLK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
7. For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit technology, 8192 refresh cycles.

REVISION HISTORY

Rev. Change Description from Previous Revision

-101 01/24/2007. Initial release. Added "U" designator to indicate that product is RoHS compliant, lead-free version.

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