

128M x 72 Bit (1GB) 184-Pin 1U Registered DIMM ECC (PC2700) 2 Rank x 8; RoHS Compliant, Lead-Free

## FEATURES

- PC2700 Compliant (DDR333B 167MHz-6ns@CL = 2.5)
- 184-Pin RDIMM form factor
- Auto and self-refresh capability (8,192 cycles/64ms refresh)
- SSTL\_2 compatible inputs and outputs
- VDD = VDDQ = 2.5V ± 0.2V
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0, /CK0) and bi-directional differential data strobe (DQS)
- Four internal component banks for concurrent operation
- Auto Precharge option for each burst access
- Data Mask (DM) for masking write data
- Burst Lengths: 2, 4, 8
- Serial Presence Detect (SPD) with EEPROM
- ECC
- Gold edge contacts
- RoHS Compliant Lead-Free

## GENERAL DESCRIPTION

The SL72E8M128M8M-B06EWU is a 128M x 72 bit (1GB) 184-pin Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Registered Dual In-line Memory Module (RDIMM) with ECC. The module uses DDR333B components and is PC2700 compliant.

The module consists of eighteen CMOS 16M x 8 bit x 4 bank DDR SDRAMs in lead-free 66-pin 400-mill TSOP-II packages mounted in 2 ranks on a 184-pin glass epoxy substrate.

A serial EEPROM using the two pin IIC protocol is also mounted to provide the Serial Presence Detects (SPD). PLL circuits supply clocks to the DDR SDRAMs. Decoupling capacitors of 0.22µF are mounted across the power supply. Damping resistors are added to the DQ, DQS, and DM signals.

All control and address signals are re-driven through a register to the DDR SDRAM devices. The control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock).

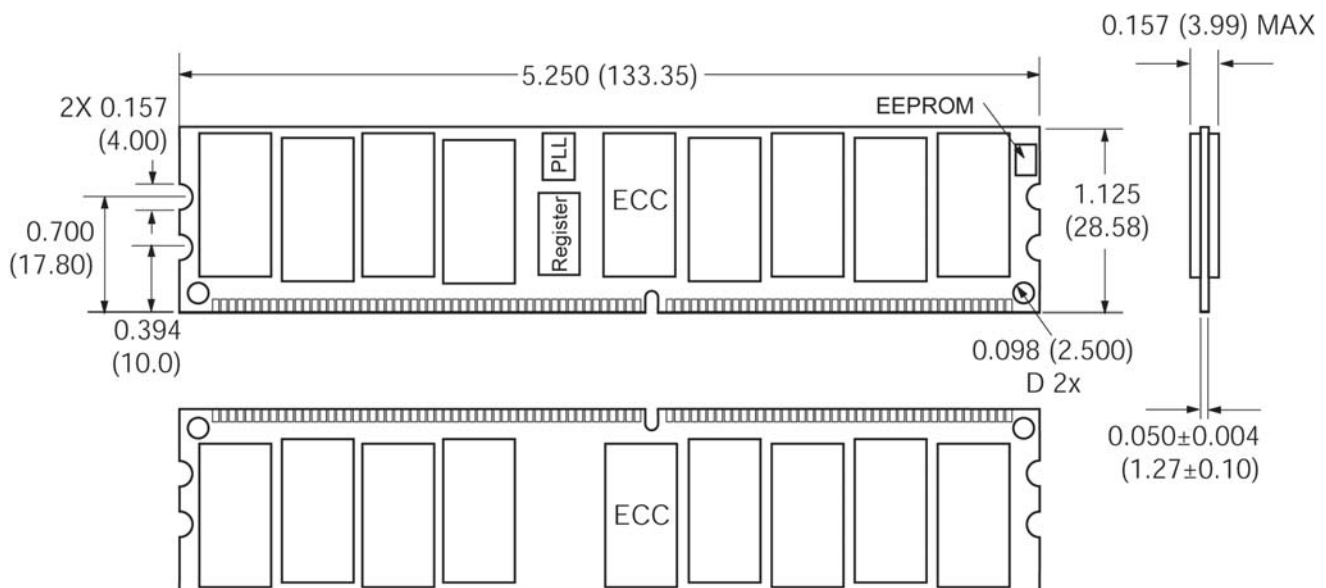
The module has gold edge connections and is intended for mounting into 184-pin DIMM edge connector sockets keyed for 2.5V VDD and VDDQ.

## ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72E8M128M8M-B06EWU	2.5	167	2.7 GB/s

## PACKAGE DIMENSIONS (Board No.: 1047)

Units are in inches (millimeters). All dimensions are typical unless otherwise specified.



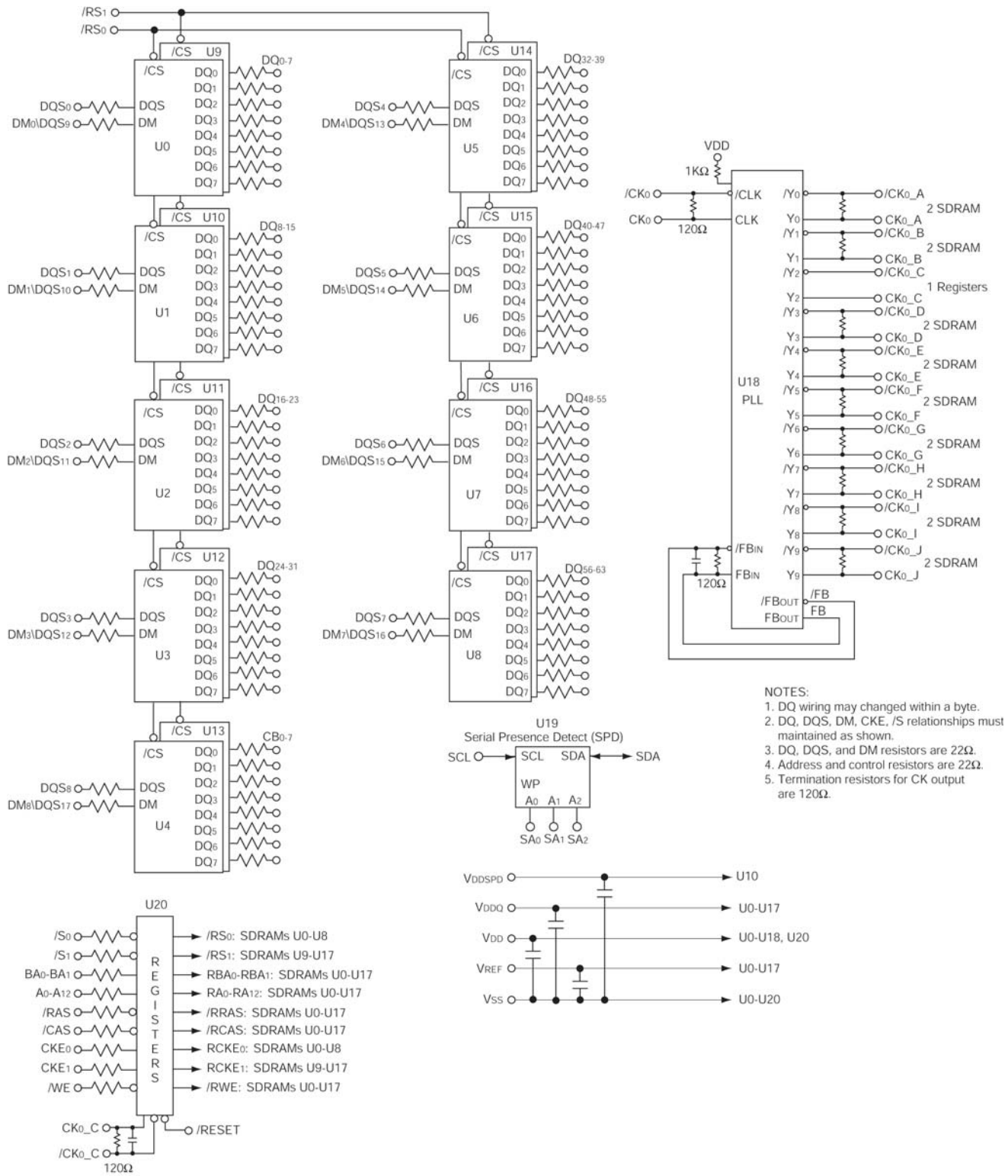
**PIN CONFIGURATION** (\* = Not Used; / = Active Low; **Bold Box** = Key)**184-PIN RDIMM PINOUT**

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	VSS	32	A5	124	VSS	62	VDDQ	154	/RAS
2	DQ0	94	DQ4	33	DQ24	125	A6	63	/WE	155	DQ45
3	VSS	95	DQ5	34	VSS	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	/CAS	157	/S0
5	DQS0	97	DM0\DQS9	36	DQS3	128	VDDQ	66	VSS	158	/S1
6	DQ2	98	DQ6	37	A4	129	DM3\DQS12	67	DQS5	159	DM5\DQS14
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	VSS
8	DQ3	100	VSS	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	VSS	70	VDD	162	DQ47
10	/RESET	102	NC	41	A2	133	DQ31	71	/S2*	163	/S3*
11	VSS	103	FETEN*	42	VSS	134	CB4	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	CB5	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	CB0	136	VDDQ	74	VSS	166	DQS3
14	DQS1	106	DQ13	45	CB1	137	CK0	75	CK2*	167	A13*
15	VDDQ	107	DM1\DQS10	46	VDD	138	/CK0	76	/CK2*	168	VDD
16	CK1*	108	VDD	47	DQS8	139	VSS	77	VDDQ	169	DM6\DQS15
17	/CK1*	109	DQ14	48	A0	140	DM8\DQS17	78	DQS6	170	DQ54
18	VSS	110	DQ15	49	CB2	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1	50	VSS	142	CB6	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	CB3	143	VDDQ	81	VSS	173	NC
21	CKE0	113	BA2*	52	BA1	144	CB7	82	VDDID*	174	DQ60
22	VDDQ	114	DQ20	<b>Key</b>				83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	VSS	84	DQ57	176	VSS
24	DQ17	116	VSS	54	VDDQ	146	DQ36	85	VDD	177	DM7\DQS16
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	VSS	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DM2\DQS11	57	DQ34	149	DM4\DQS13	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	VSS	150	DQ38	89	VSS	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	VDDQ	122	A8	60	DQ35	152	VSS	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

**PIN CONFIGURATION** *(Continued)***PIN FUNCTIONS**

<b>Symbol</b>	<b>Description</b>
A0-A11, A12, A13*	SDRAM Address Bus
BA0-BA1, BA2*	SDRAM Bank Select
DQ0-DQ63	DIMM Memory Data Bus
CB0-CB7	DIMM ECC Check Bits
/RAS	SDRAM Row Address Strobe
/CAS	SDRAM Column Address Strobe
/WE	SDRAM Write Strobe
/S0, /S1, /S2*, /S3*	SDRAM Chip Select Lines (Physical Banks 0, 1, 2, and 3)
CKE0, CKE1	SDRAM Clock Enable Lines
DQS0-DQS8	SDRAM Low Data Strobes
DM(0-8)\DQS(9-17)	SDRAM Low Data Masks\High Data Strobes (x4, x8-based x72 DIMMs)
VDDID*	VDD Identification Flag
CK0, CK1*, CK2*	SDRAM Clock (Positive Line of Differential Pair)
/CK0, /CK1*, /CK2*	SDRAM Clock (Negative Line of Differential Pair)
SCL	IIC Serial Bus Clock for EEPROM
SDA	IIC Serial Bus Data Line for EEPROM
SA0-SA2	IIC Slave Address Select for EEPROM
VDD	SDRAM Positive Power Supply
VDDQ	SDRAM I/O Driver Positive Power Supply
VREF	SDRAM I/O Reference Supply
VSS	Power Supply Return (Ground)
VDDSPD	Serial EEPROM Positive Power Supply (2.2V <= VDDSPD <= 5.5V)
NC	Spare Pins (No Connect)
/RESET	Reset Pin (Forces Register Inputs Low)
FETEN*	FET Enable Line

## FUNCTIONAL BLOCK DIAGRAM



- NOTES:**
1. DQ wiring may be changed within a byte.
  2. DQ, DQS, DM, CKE, /S relationships must be maintained as shown.
  3. DQ, DQS, and DM resistors are 22Ω.
  4. Address and control resistors are 22Ω.
  5. Termination resistors for CK output are 120Ω.

**SERIAL PRESENCE DETECT INFORMATION**

Serial PD Interface Protocol: I2C; Current sink capability of SDA driver  $\leq 3\text{mA}$ ; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
0	Number of SPD Bytes used by Manufacturer	128	80h
1	Total Number of Bytes in SPD Device	256	08h
2	Fundamental Memory Type	DDR SDRAM	07h
3	Number of Row Addresses on Assembly	13	0Dh
4	Number of Column Addresses on Assembly	11	0Bh
5	Number of Ranks on Assembly	2	02h
6	Module Data Width	72	48h
7	Reserved	Undefined	00h
8	Module Voltage Interface Levels	SSTL 2.5V	04h
9	SDRAM Cycle Time, tCYC(min), CL = 2.5	6.0ns	60h
10	SDRAM Access Time from Clock, tAC(max), CL = 2.5	+/-0.70ns	70h
11	Module Configuration Type	ECC	02h
12	Refresh Rate/Type	7.8 $\mu$ s/SELF	82h
13	SDRAM Device Width (Primary SDRAM)	x8	08h
14	Error-checking SDRAM Data Width	x8	08h
15	Minimum Clock Delay, Back-to-Back Random Column Addressing	tCCD = 1CLK	01h
16	Burst Lengths Supported	2, 4, 8	0Eh
17	Number of Banks on SDRAM Device	4	04h
18	CAS Latencies Supported	2, 2.5	0Ch
19	CS Latencies Supported	0	01h
20	Write Latency	1	02h
21	SDRAM Module Attributes	1 Register/1PLL Differential Clock	26h
22	SDRAM Device Attributes: General	Vdd +/- 0.2V	00h
23	Minimum Clock Cycle Time at CL X-1, CL = 2, tCYC(min)	7.5ns	75h
24	Minimum Data Access Time from Clock at CL X-1, CL = 2, tAC(max)	+/-0.70ns	70h
25	Minimum Clock Cycle Time at CL X-2	N/A	00h
26	Maximum Data Access Time from Clock at CL X-2	N/A	00h
27	Minimum Row Precharge Time, tRP	18ns	48h
28	Minimum Row Active to Row Active, tRRD	12ns	30h
29	Minimum /RAS to /CAS Delay, tRCD	18ns	48h
30	Minimum /RAS Pulse Width, tRAS	42ns	2Ah
31	Module Rank Density	512MB	80h
32	Address and Command Signal Setup Time, tAS(min)	0.75ns	75h
33	Address and Command Signal Hold Time, tAH(min)	0.75ns	75h
34	Data Signal Input Setup Time, tDS(min)	0.45ns	45h
35	Data Signal Input Hold Time, tDH(min)	0.45ns	45h
36 - 40	Reserved for VCSDRAM (Virtual Channel SDRAM)	-	00h

(Serial Presence Detect Information continued on next page.)

**SERIAL PRESENCE DETECT INFORMATION** *(continued)*

Byte	Description	Entry	Hex Value
41	Min. Active Auto Refresh Time, tRC	60ns	3Ch
42	Min. Auto Refresh to Active/Auto Refresh Command Period, tRFC	72ns	48h
43	SDRAM Device Max. Cycle Time, tCKMAX	12ns	30h
44	SDRAM Device Max. DQS-DQ Skew Time, tDQSQ	0.45ns	2Dh
45	SDRAM Device Max. Read Data Hold Skew Factor, tQHS	0.55ns	55h
46-61	Superset Information (Reserved for Future Use)	-	00h
62	SPD Revision	JEDEC Intial Release	00h
63	Checksum for Bytes 0 - 62	1946/256=7R154	9Ah
64	Manufacturer's JEDEC ID Code SimpleTech	Continuation Code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71	—	—	00h
72	Manufacturing Location	STEC USA	01h
73-90	Module Part Number (ASCII)	—	00h
91	Module Revision Code	Engineering (00) Rev. A (01) Rev. B (02)	00h
92	—	—	00h
93	Year of Manufacture (BCD)	1998 = 98h	98h
94	Week of Manufacture (BCD)	Week 12 = 12h	12h
95	Module Serial Number	Tester Number	ssh
96		Serial # (Bits 7-0)	ssh
97		Serial # (Bits 15-8)	ssh
98		Serial # (Bits 23-16)	ssh
99-108	Manufacturer-Specific Data (RSVD)	S	53h
		i	69h
		m	6Dh
		p	70h
		l	6Ch
		e	65h
		T	54h
		e	65h
		c	63h
		h	68h
109-127	None	-	00h
128-255	Open for Customer Use	-	00h

## ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to higher than recommended voltages for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
VIN, VOUT	Voltage on any Pin Relative to VSS	-0.5	+3.6	V
VDD	Voltage on VDD Supply Relative to VSS	-1.0	+3.6	V
VDDQ	Voltage on VDDQ Supply Relative to VSS	-1.0	+3.6	V
PD	Power Dissipation	18		W
IOS	Short Circuit Current	50		mA
TSTG	Storage Temperature	-55	+150	°C

## POWER and DC OPERATING CONDITIONS (SSTL\_2 IN/OUT)

Recommended Operating Conditions (Voltage referenced to VSS = 0V. TA = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Supply Voltage (for device with a nominal VDD of 2.5V)	2.3	2.7	V	
VDDQ	I/O Supply Voltage	2.3	2.7	V	
VREF	I/O Reference Voltage	VDDQ/2-50mV	VDDQ/2+50mV	V	1
VTT	I/O Termination Voltage (System)	VREF-0.04	VREF+0.04	V	2
VIH(DC)	Input Logic High Voltage	VREF+0.15	VDDQ+0.3	V	4
VIL(DC)	Input Logic Low Voltage	-0.3	VREF-0.15	V	4
VIN(DC)	Input Voltage Level, CK and /CK	-0.3	VDDQ+0.3	V	
VID(DC)	Input Differential Voltage, CK and /CK	0.3	VDDQ+0.6	V	3
VIX(DC)	Input Crossing Point Voltage, CK and /CK	1.15	1.35	V	5
IL	Input Leakage Current	-5	5	µA	
IOZ	Output Leakage Current	-10	10	µA	
IOH	Output High Current (VOUT=VTT+0.84V) (Normal Strength Driver)	-16.8		mA	
IOL	Output Low Current (VOUT=VTT-0.84V) (Normal Strength Driver)	16.8		mA	
IOH	Output High Current (VOUT=VTT+0.45V) (Half Strength Driver)	-9		mA	
IOL	Output Low Current (VOUT=VTT-0.45V) (Normal strength driver)	9		mA	

### Notes:

- Includes  $\pm 25\text{mV}$  margin for DC offset on VREF, and a combined total of  $\pm 50\text{mV}$  margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in V REF noise. VREF should be de-coupled with an inductance of  $\leq 3\text{nH}$ .
- V TT is not applied directly to the device. V TT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
- VID is the magnitude of the difference between the input level on CK and the input level on /CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
- The value of VIX is expected to equal  $0.5 \cdot \text{VDDQ}$  of the transmitting device and must track variations in the dc level of the same.
- These characteristics obey the SSTL-2 class II standards.

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted. VDD=2.7, T=10°C; Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.)

Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; tRC = tRC(MIN); tCK = tCK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;	IDD0	1,215	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOU = 0mA; Address and control inputs changing once per clock cycle	IDD1	1,485	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; tCK = tCK (MIN); CKE = (LOW)	IDD2P	90	mA
IDLE STANDBY CURRENT: CS# = HIGH; All banks idle; tCK = tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	450	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW	IDD3P	360	mA
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank; Active-Precharge; tRC = tRAS(MAX); tCK = tCK(MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	495	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK(MIN); IOU = 0mA	IDD4R	1,530	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	1,620	mA
AUTO REFRESH CURRENT: tRC = tRC(MIN)	IDD5	2,655	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V	IDD6	90	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, tRC = tRC(MIN); tCK = tCK(MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7	3,690	mA

## AC OPERATING CONDITIONS

(VDD = VDDQ = 2.5V, TA = 25°C, f = 1MHz.)

Symbol	Parameter/Condition	Min	Max	Units	Note
VIH(AC)	Input High (Logic 1) Voltage, DQ, DQS, and DM signals	VREF+0.31		V	3
VIL(AC)	Input Low (Logic 0) Voltage, DQ, DQS, and DM signals		VREF-0.31	V	3
VID(AC)	Input Differential Voltage, CK and /CK inputs	0.7	VDDQ+0.6	V	1
VIX(AC)	Input Crossing Point Voltage, CK and /CK inputs	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

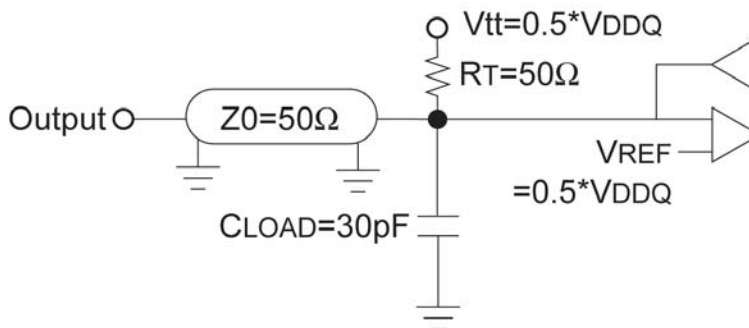
### Notes:

- VID is the magnitude of the difference between the input level on CK and the input on /CK.
- The value of VIX is expected to equal 0.5\*V DDQ of the transmitting device and must track variations in the DC level of the same.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a Vref envelope that has been bandwidth limited 20MHz.

**AC OPERATING TEST CONDITIONS**

(VDD = VDDQ = 2.5V, TA = 25°C, f = 1MHz.)

Parameter	Value	Unit
Input Reference Voltage for Clock	0.5*VDDQ	V
Input Signal Maximum Peak Swing	1.5	V
Input Signal Minimum Slew Rate	0.5	V/ns
Input Levels (VIH/VIL)	VREF+0.31/VREF-0.31	V
Input Timing Measurement Reference Level	VREF	V
Output Timing Measurement Reference Level	VTT	V
Output Load Condition	See Output Load Circuit (SSTL_2)	



Output Load Circuit (SSTL\_2)

**INPUT/OUTPUT CAPACITANCE**

(VDD = VDDQ = 2.5V, TA = 25°C, f = 1MHz.)

Symbol	Parameter	Max	Units
CIN1	Input Capacitance (A0-A12, BA0, BA1, /RAS, /CAS, /WE)	15	pF
CIN2	Input Capacitance (CKE0, CKE1)	15	pF
CIN3	Input Capacitance (/S0, /S1)	15	pF
CIN4	Input Capacitance (CK0, /CK0)	15	pF
CIN5	Input Capacitance (DM0\DQS9-DM8\DQS17, DQS0-DQS8)	15	pF
COUT1	Data Input/Output Capacitance (DQ0-DQ63)	15	pF
COUT2	Data Input/Output Capacitance (CB0-CB7)	15	pF

## AC TIMING PARAMETERS

Note: These AC characteristics were tested on the component.

Parameter	Symbol	Min	Max	Units
Access Window of DQs from CK, /CK	tAC	-0.7	0.7	ns
CK High-Level Width	tCH	0.45	0.55	tCK
CK Low-Level Width	tCL	0.45	0.55	tCK
Clock Cycle Time	CL = 2.5 tCK (2.5)	6	12	ns
	CL = 2 tCK (2)	7.5	12	ns
DQ and DM Input Hold Time Relative to DQS	tDH	0.45		ns
DQ and DM Input Setup Time Relative to DQS	tDS	0.45		ns
DQ and DM Input Pulse Width (for each input)	tDIPW	1.75		ns
Access Window of DQS from CK, /CK	tDQSK	-0.6	0.6	ns
DQS Input High Pulse Width	tDQSH	0.35		tCK
DQS Input Low Pulse Width	tDQSL	0.35		tCK
DQS-DQ skew, DQS to Last DQ Valid, Per Group, Per Access	tDQSQ		0.45	ns
Write Command to First DQS Latching Transition	tDQSS	0.75	1.25	CK
DQS Falling Edge to CK Rising - Setup Time	tDSS	0.2		tCK
DQS Falling Edge from CK Rising - Hold Time	tDSH	0.2		tCK
Half Clock Period	tHP	tCH, tCL		ns
Data-out High-Impedance Window from CK, /CK	tHZ	-0.7	0.7	ns
Data-out Low-Impedance Window from CK, /CK#	tLZ	-0.7	0.7	ns
Address and Control Input Hold Time (fast slew rate)	tIHF	0.75		ns
Address and Control Input Setup Time (fast slew rate)	tISF	0.75		ns
Address and Control Input Hold Time (slow slew rate)	tIHS	0.8		ns
Address and Control Input Setup Time (slow slew rate)	tISS	0.8		ns
Address and Control Input Pulse Width	tIPW	2.2		ns
LOAD MODE REGISTER Command Cycle Time	tMRD	12		ns
DQ-DQS Hold, DQS to First DQ to go Non-Valid, Per Access	tQH	tHP - tQHS		ns
Data Hold Skew Factor	tQHS		0.55	ns
ACTIVE to AUTOPRECHARGE Command	tRAP	18		ns
ACTIVE to PRECHARGE Command	tRAS	42	70,000	ns
ACTIVE to ACTIVE/AUTO REFRESH Command Period	tRC	60		ns
AUTO REFRESH Command Period	tRFC	72		ns
ACTIVE to READ or WRITE Delay	tRCD	18		ns
PRECHARGE Command Period	tRP	18		ns
DQS Read Preamble	tRPRE	0.9	1.1	tCK
DQS Read Postamble	tRPST	0.4	0.6	tCK
ACTIVE Bank a to ACTIVE Bank b Command	tRRD	12		ns
DQS Write Preamble	tWPRE	0.25		tCK
DQS Write Preamble Setup Time	tWPRES	0		ns
DQS Write Postamble	tWPST	0.4	0.6	tCK
Write Recovery Time	tWR	15		ns
Internal WRITE to READ Command Delay	tWTR	1		t CK
Data Valid Output Window	N/A	t QH - tDQSQ		ns
REFRESH to REFRESH Command Interval	tREFC	70.3		µs
Average Periodic Refresh interval	tREFI	7.8		µs
Terminating Voltage Delay to VDD	tVTD	0		ns
Exit SELF REFRESH to Non-READ Command	tXSNR	75		ns
Exit SELF REFRESH to READ Command	tXSRD	200		tCK

## REVISION HISTORY

### Rev. Change Description from Previous Revision

-101 01/31/2007. Initial release.

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