

32M x 72 Bit (256MB) 184-Pin Unbuffered DIMM ECC (PC2100) 1 Rank x 8; RoHS Compliant, Lead-Free

FEATURES

- PC2100 Compliant (DDR266B 133MHz-7.5ns@CL = 2.5)
- 184-Pin DIMM form factor
- Auto and Self-Refresh capability (8,192 cycles/64ms refresh)
- VDD = VDDQ = 2.5V ± 0.2V
- SSTL_2 compatible inputs and outputs
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0, /CK0), bi-directional differential data strobe (DQS)
- Four internal component banks for concurrent operation
- Burst Lengths: 2, 4, 8
- Serial Presence Detect (SPD) with EEPROM
- ECC
- Gold edge contacts
- RoHS Compliant Lead-Free

GENERAL DESCRIPTION

The SL72C8F32M8M-B75EWU is a 32M x 72 bit (256MB) 184-pin Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Unbuffered Dual In-line Memory Module (UDIMM) with data ECC.

The module consists of nine CMOS 8M x 8 bit x 4 bank DDR266B SDRAMs in lead-free 66-pin 400-mil TSOP-II packages mounted in 1 rank on a 184-pin glass epoxy substrate.

A serial EEPROM using the two pin I²C protocol is also mounted to provide the Serial Presence Detects (SPD). Decoupling capacitors of 0.22µF are also mounted. Damping resistors are added in series for DQ, DQS, and DM signals.

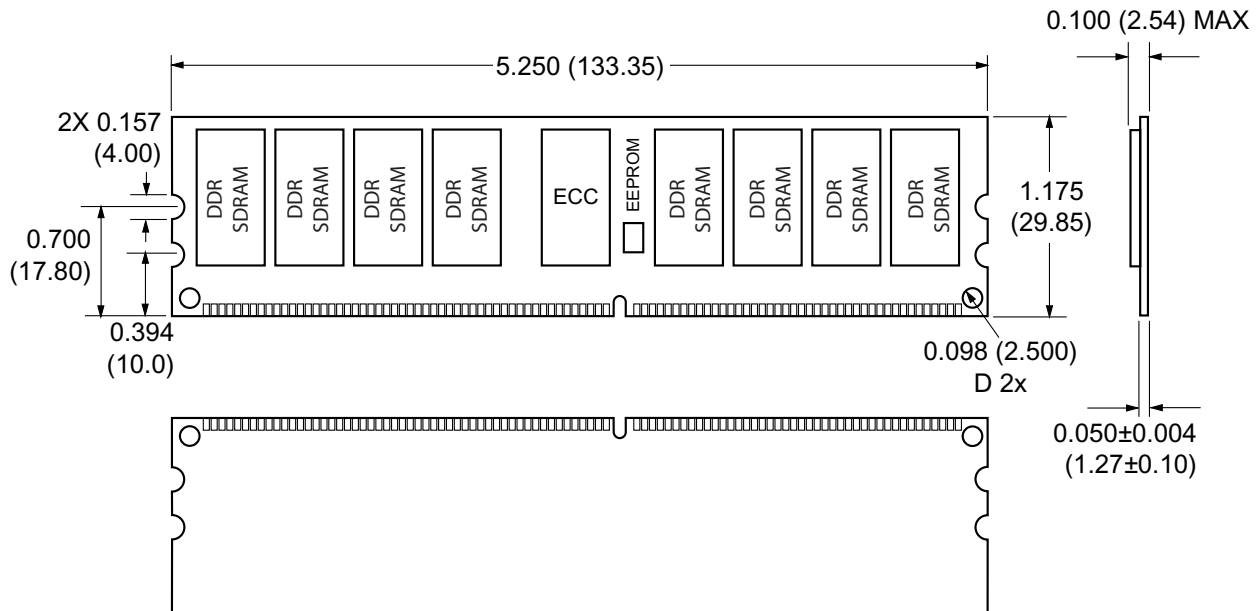
The module has gold edge connections and is intended for mounting into 184-pin DIMM edge connector sockets keyed for 2.5V.

ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72C8F32M8M-B75EWU	2.5	133	2.1 GB/s

PACKAGE DIMENSIONS (Board No.: 1077)

Units are in inches (millimeters). All dimensions are typical unless otherwise specified.



PIN CONFIGURATION (* = Not Used; / = Active Low; **Bold Box** = Key)

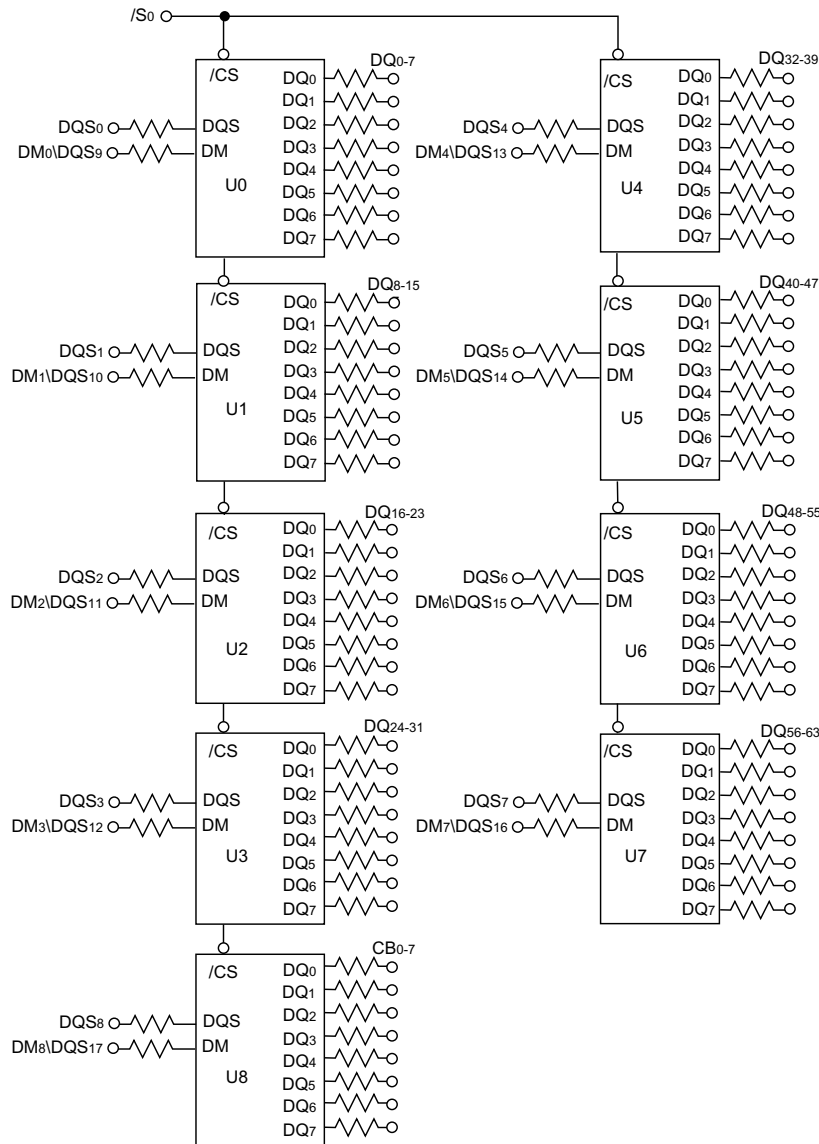
184-PIN UDIMM PINOUT

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	VSS	32	A5	124	VSS	62	VDDQ	154	/RAS
2	DQ0	94	DQ4	33	DQ24	125	A6	63	/WE	155	DQ45
3	VSS	95	DQ5	34	VSS	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	/CAS	157	/S0
5	DQS0	97	DM0\DQS9	36	DQS3	128	VDDQ	66	VSS	158	/S1*
6	DQ2	98	DQ6	37	A4	129	DM3\DQS12	67	DQS5	159	DM5\DQS14
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	VSS
8	DQ3	100	VSS	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	VSS	70	VDD	162	DQ47
10	/RESET*	102	NC	41	A2	133	DQ31	71	/S2*	163	/S3*
11	VSS	103	A13*	42	VSS	134	CB4	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	CB5	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	CB0	136	VDDQ	74	VSS	166	DQS3
14	DQS1	106	DQ13	45	CB1	137	CK0	75	CK2	167	FETEN*
15	VDDQ	107	DM1\DQS10	46	VDD	138	/CK0	76	/CK2	168	VDD
16	CK1	108	VDD	47	DQS8	139	VSS	77	VDDQ	169	DM6\DQS15
17	/CK1	109	DQ14	48	A0	140	DM8\DQS17	78	DQS6	170	DQ54
18	VSS	110	DQ15	49	CB2	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1*	50	VSS	142	CB6	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	CB3	143	VDDQ	81	VSS	173	NC
21	CKE0	113	BA2*	52	BA1	144	CB7	82	VDDID*	174	DQ60
22	VDDQ	114	DQ20	Key		Key		83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	VSS	84	DQ57	176	VSS
24	DQ17	116	VSS	54	VDDQ	146	DQ36	85	VDD	177	DM7\DQS16
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	VSS	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DM2\DQS11	57	DQ34	149	DM4\DQS13	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	VSS	150	DQ38	89	VSS	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	VDDQ	122	A8	60	DQ35	152	VSS	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

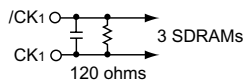
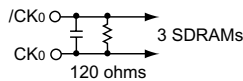
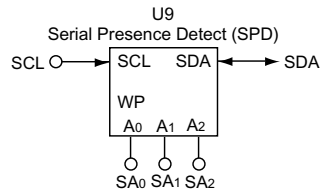
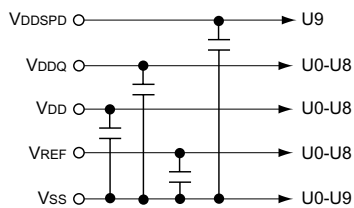
PIN FUNCTIONS

Symbol	Description	Symbol	Description
A0-A11, A12, A13*	SDRAM Address Bus	/CK0, /CK1, /CK2	SDRAM Clock (Negative Line of Differential Pair)
BA0-BA1, BA2*	SDRAM Bank Select		
DQ0-DQ63	DIMM Memory Data Bus	SCL	IIC Serial Bus Clock for EEPROM
CB0-CB7	DIMM ECC Check Bits	SDA	IIC Serial Bus Data Line for EEPROM
/RAS	SDRAM Row Address Strobe	SA0-SA2	IIC Slave Address Select for EEPROM
/CAS	SDRAM Column Address Strobe	VDD	SDRAM Positive Power Supply
/WE	SDRAM Write Strobe	VDDQ	SDRAM I/O Driver Positive Power Supply
/S0, /S1*, /S2*, /S3*	SDRAM Chip Select Lines (Physical Banks 0, 1, 2 and 3)	VREF	SDRAM I/O Reference supply
CKE0, CKE1*	SDRAM Clock Enable Lines	VSS	Power Supply Return (Ground)
DQS0-DQS8	SDRAM Low Data Strokes	VDDSPD	Serial EEPROM Positive Power Supply (2.5 volts)
DM(0-8)\DQS(9-17)	SDRAM Low Data Masks\High Data Strokes (x4, x8-based x72 DIMMs)	NC	Spare Pins (No Connect)
VDDID*	VDD Identification flag	/RESET*	Reset Pin (Forces Register Inputs Low)
CK0, CK1, CK2	SDRAM Clock (Positive Line of Differential Pair)	FETEN*	FET Enable Line

FUNCTIONAL BLOCK DIAGRAM



BA0-BA1 → BA0-BA1: SDRAMs U0-U8
 A0-A12 → A0-A12: SDRAMs U0-U8
 /RAS → /RAS: SDRAMs U0-U8
 /CAS → /CAS: SDRAMs U0-U8
 CKE0 → CKE0: SDRAMs U0-U8
 /WE → /WE: SDRAMs U0-U8



- Notes:
1. DQ wiring may be changed within a byte.
 2. DQ, DQS, DM, CKE, /S relationships must be maintained as shown.
 3. DQ, DQS, and DM resistors are 22 ohms.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I2C; Current sink capability of SDA driver $\leq 3\text{mA}$; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
0	Number of SPD Bytes used by Manufacturer	128	80h
1	Total Number of Bytes in SPD Device	256	08h
2	Fundamental Memory Type	DDR SDRAM	07h
3	Number of Row Addresses on Assembly	13	0Dh
4	Number of Column Addresses on Assembly	10	0Ah
5	Module Ranks on Assembly	1	01h
6	Module Data Width	72	48h
7	Module Data Width (Continued)	-	00h
8	Module Voltage Interface Levels	SSTL 2.5V	04h
9	SDRAM Cycle Time, tCYC(min) (CAS Latency = 2.5)	7.5ns	75h
10	SDRAM Access from Clock, tAC(max) (CAS Latency = 2.5)	+/-0.75ns	75h
11	Module Configuration Type	ECC	02h
12	Refresh Rate/Type	7.8 μ s/SELF	82h
13	SDRAM Device Width (Primary SDRAM)	x8	08h
14	Error-checking SDRAM Data Width	x8	08h
15	Min. Clock Delay, Back-to-Back Rand. Col. Addr., tCCD	1 CLK	01h
16	Burst Lengths Supported	2, 4, 8	0Eh
17	Number of Banks on SDRAM Device	4	04h
18	CAS Latencies Supported	2, 2.5	0Ch
19	CS Latencies Supported	0	01h
20	Write Latency	1	02h
21	SDRAM Module Attributes	Differential Clock	20h
22	SDRAM Device Attributes: General	Vdd +/-0.2V	00h
23	Minimum Clock Cycle Time at CL X-1, CL = 2, tCYC(min)	10ns	A0h
24	Maximum Data Access Time from Clock at CL X-1, tAC(max)	+/-0.75ns	75h
25	Minimum Clock Cycle Time at CL X-2	N/A	00h
26	Maximum Data Access Time from Clock at CL X-2	N/A	00h
27	Minimum Row Precharge Time, tRP(min)	20ns	50h
28	Minimum Row Active to Row Active Delay, tRRD(min)	15ns	3Ch
29	Minimum /RAS to /CAS Delay, tRCD(min)	20ns	50h
30	Minimum /RAS Pulse Width, tRAS(min)	45ns (Samsung)	2Dh
31	Module Rank Density	256MB	40h
32	Command and Address Setup Time, tAS(min)	0.9ns	90h
33	Command and Address Hold Time, tAH(min)	0.9ns	90h
34	Data Signal Input Setup Time, tDS(min)	0.5ns	50h
35	Data Signal Input Hold Time, tDH(min)	0.5ns	50h
36 - 40	Reserved for Virtual Channel SDRAM (VCSDRAM)	-	00h

(Serial Presence Detect Information continued on next page.)

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte	Description	Entry	Hex Value
41	Minimum Active/Auto-Refresh Time, tRC(min)	65ns	41h
42	Min. Auto Refresh to Active/Auto Refresh Command Period, tRFC	75ns	4Bh
43	SDRAM Device Max. Cycle Time, tCK(max)	13ns (Micron)	34h
44	SDRAM Device Max. DQS-DQ Skew Time, tDQSQ(max)	0.50ns	34h
45	SDRAM Device Max. Read Data Hold Skew Factor, tQHS(max)	0.75ns	75h
46 - 61	Superset Information (Reserved for Future Use)	-	00h
62	SPD Revision	JEDEC Initial Initial Release	00h
63	Checksum for Bytes 0 - 62	2104/256=8R56	38h
64	Manufacturer's JEDEC ID Code per JEP-106E	Continuation Code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71	—	—	00h
72	Manufacturing Location	STEC USA	01h
73-90	Module Part Number (ASCII)	—	00h
91	Module Revision Code	Engineering (00) Rev. A (01) Rev. B (02)	00h
92	—	—	00h
93	Year of Manufacture (BCD)	1998 = 98h	98h
94	Week of Manufacture (BCD)	Week 12 = 12h	12h
95	Module Serial Number	Tester Number	ssh
96		Serial # (Bits 7-0)	ssh
97		Serial # (Bits 15-8)	ssh
98		Serial # (Bits 23-16)	ssh
99	Manufacturer-Specific Data (RSVD)	S	53h
100		T	54h
101		E	45h
102		C	43h
103-127	None	-	00h
128-255	Open for Customer Use	-	00h

ABSOLUTE MAXIMUM DC RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to higher than recommended voltages for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
VIN, VOUT	Voltage on any Pin Relative to VSS	-0.5	+3.6	V
VDD	Voltage on VDD Supply Relative to VSS	-1.0	+3.6	V
VDDQ	Voltage on VDDQ Supply Relative to VSS	-1.0	3.6	V
TSTG	Storage Temperature	-55	+150	°C
PD	Power Dissipation	13.5		W
IOS	Short Circuit Current	50		mA

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

Recommended Operating Conditions. Voltage referenced to VSS = 0V, TA = 0 to 70°C.

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Supply Voltage (For Device with a Nominal VDD of 2.5V)	2.3	2.7	V	
VDDQ	I/O Supply Voltage	2.3	2.7	V	
VREF	I/O Reference Voltage	VDDQ/2-50mV	VDDQ/2+50mV	V	1
VTT	I/O Termination Voltage (System)	VREF-0.04	VREF+0.04	V	2
VIH(DC)	Input Logic High Voltage	VREF+0.15	VDDQ+0.3	V	4
VIL(DC)	Input Logic Low Voltage	-0.3	VREF-0.15	V	4
VIN(DC)	Input Voltage Level, CK and /CK	-0.3	VDDQ+0.3	V	
VID(DC)	Input Differential Voltage, CK and /CK	0.3	VDDQ+0.6	V	3
VIX(DC)	Input Crossing Point voltage, CK and /CK	1.15	1.35	V	5
IL	Input Leakage Current	-18	18	µA	
IOZ	Output Leakage current	-5	5	µA	
IOH	Output High Current (VOUT = VTT+0.84V) (Normal Strength driver)	-16.8		mA	
IOL	Output Low Current (VOUT = VTT-0.84V) (Normal Strength Driver)	16.8		mA	
IOH	Output High Current (VOUT = VTT+0.45V) (Half Strength Driver)	-9		mA	
IOL	Output Low Current (VOUT = VTT-0.45V) (Normal Strength Driver)	9		mA	

Notes:

- Includes $\pm 25\text{mV}$ margin for DC offset on VREF, and a combined total of $\pm 50\text{mV}$ margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in V REF noise. VREF should be de-coupled with an inductance of $\leq 3\text{nH}$.
- V TT is not applied directly to the device. V TT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
- VID is the magnitude of the difference between the input level on CK and the input level on /CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
- The value of VIX is expected to equal $0.5 \cdot \text{VDDQ}$ of the transmitting device and must track variations in the dc level of the same.
- These characteristics obey the SSTL-2 class II standards.

DC CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted. Module IDD was calculated on the basis of the component IDD and can be measured differently according to DQ loading capacity.

Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; tRC = tRC(MIN); tCK = tCK(MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;	IDD0	1,080	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; tRC = tRC(MIN); tCK = tCK(MIN); IOU = 0mA; Address and control inputs changing once per clock cycle	IDD1	1,305	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; tCK = tCK(MIN); CKE = (LOW)	IDD2P	36	mA
IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; tCK = tCK(MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	405	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; tCK = tCK(MIN); CKE = LOW	IDD3P	270	mA
ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; tRC = tRAS(MAX); tCK = tCK(MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	450	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK(MIN); IOU = 0mA	IDD4R	1,350	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK(MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	1,350	mA
AUTO REFRESH CURRENT: tRC = tRC(MIN)	IDD5	54	mA
SELF REFRESH CURRENT: CKE <= 0.2V	IDD6	36	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, tRC = tRC(MIN); tCK = tCK(MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7	3,285	mA

AC OPERATING CONDITIONS

VDD = VDDQ = 2.5V, TA = 25°C, f = 1MHz.

Symbol	Parameter/Condition	Min	Max	Units	Note
VIH(AC)	Input High (Logic 1) Voltage: DQ, DQS and DM Signals	VREF+0.31		V	3
VIL(AC)	Input Low (Logic 0) Voltage: DQ, DQS and DM Signals		VREF-0.31	V	3
VID(AC)	Input Differential Voltage: CK and /CK Inputs	0.7	VDDQ+0.6	V	1
VIX(AC)	Input Crossing Point Voltage: CK and /CK Inputs	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

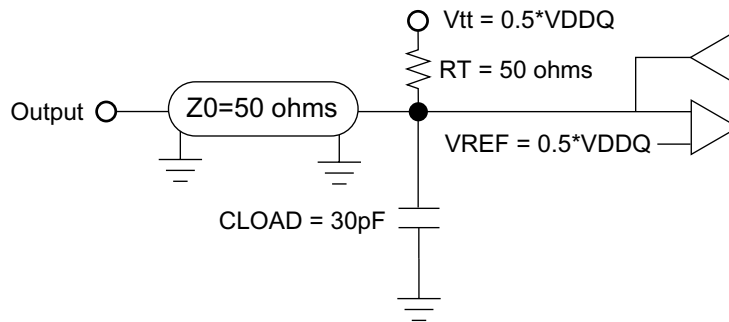
Notes:

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on the actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are in relation to a VREF envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS

VDD = VDDQ = 2.5V, TA = 25°C, f = 1MHz.

Parameter	Value	Unit
Input Reference Voltage for Clock	0.5*VDDQ	V
Input Signal Maximum Peak Swing	1.5	V
Input Signal Minimum Slew Rate	0.5	V/ns
Input Levels (VIH/VIL)	VREF+0.31/VREF-0.31	V
Input Timing Measurement Reference Level	VREF	V
Output Timing Measurement Reference Level	VTT	V
Output Load Condition	See Output Load Circuit	



Output Load Circuit (SSTL_2)

INPUT/OUTPUT CAPACITANCE

VDD = VDDQ = 2.5V, TA = 25°C, f = 1MHz.

Symbol	Parameter	Max	Units
CIN1	Input Capacitance: A0-A12, BA0, BA1, /RAS, /CAS, /WE	37	pF
CIN2	Input Capacitance: CKE0	37	pF
CIN3	Input Capacitance: /S0	37	pF
CIN4	Input Capacitance: CK0-CK3	14	pF
COUT	Data and DQS I/O Capacitance: DQ0-DQ63, CB0-CB7, DQS0-DQS17	15	pF
CIN5	Input Capacitance: DM0-DM8	15	pF

AC TIMING PARAMETERS (These AC Characteristics were tested on the component.)

		DDR266B			
Symbol	Parameter	Min	Max	Unit	Notes
tRC	Row Cycle Time	65		ns	
tRFC	Refresh Row Cycle Time	75		ns	
tRAS	Row Active Time	45	120K	ns	
tRCD	/RAS to /CAS Delay	20		ns	
tRP	Row Precharge Time	20		ns	
tRRD	Row Active to Row Active Delay	15		ns	
tWR	Write Recovery Time	15		ns	
tWTR	Last Data In to READ Command	1		tCK	
tCCD	Column Address to Column Address Delay	1		tCK	
tCK	Clock Cycle Time, CL = 2.0	10	12	ns	5
	Clock Cycle Time, CL = 2.5	7.5	12	ns	5
tCH	Clock High Level Width	0.45	0.55	tCK	
tCL	Clock Low Level Width	0.45	0.55	tCK	
tDQSCK	DQS-Out Access Time from CK, /CK	-0.75	+0.75	ns	
tAC	Output Data Access Time from CK, /CK	-0.75	+0.75	ns	
tDQSQ	Data Strobe Edge to Output Data Edge	-	0.5	ns	5
tRPRE	Read Preamble	0.9	1.1	tCK	
tRPST	Read Postamble	0.4	0.6	tCK	
tDQSS	CK to Valid DQS-In	0.75	1.25	tCK	
tWPRES	DQS-In Setup Time	0		ns	2
tWPRE	DQS-In Hold Time	0.25		tCK	
tDSS	DQS Falling Edge to CK Rising - Setup Time	0.2		tCK	
tDSH	DQS Falling Edge to CK Rising - Hold Time	0.2		tCK	
tDQSH	DQS-In High Level Width	0.35		tCK	
tDQSL	DQS-In Low Level Width	0.35		tCK	
tDSC	DQS-In Cycle Time	0.9	1.1	tCK	
tIS	Address and Control Input Setup Time (Fast)	0.9		ns	6
tIH	Address and Control Input Hold Time (Fast)	0.9		ns	6
tIS	Address and Control Input Setup Time (Slow)	1.0		ns	6
tIH	Address and Control Input Hold Time (Slow)	1.0		ns	6
tHZ	Data-Out High Impedance Time from CK, /CK	-0.75	+0.75	ns	
tLZ	Data-Out Low Impedance Time from CK, /CK	-0.75	+0.75	ns	
tSL(I)	Input Slew Rate, Input Pins	0.5		V/ns	6
tSL(IO)	Input Slew Rate, I/O Pins	0.5		V/ns	7
tSL(O)	Input Slew Rate, x4, x8 Devices	1.0	4.5	V/ns	10
tSLMR	Output Slew Rate Matching Ratio (Rise to Fall)	0.67	1.5		

(AC Timing Parameters continued on next page.)

AC TIMING PARAMETERS *(continued)*

Symbol	Parameter	DDR266B		Unit	Notes
		Min	Max		
tMRD	Mode Register Set Cycle Time	15		ns	
tDS	DQ and DM Setup Time to DQS	0.5		ns	7, 8, 9
tDH	DQ and DM Hold Time to DQS	0.5		ns	7, 8, 9
tIPW	Control and Address Input Pulse Width	2.2		ns	
tDIPW	DQ and DM Input Pulse Width	1.75		ns	
tPDEX	Power Down Exit Time	7.5		ns	
tXSNR	Exit Self-Refresh to Non-READ Command	75		ns	4
tXSRD	Exit Self-Refresh to READ Command	200		tCK	
tREFI	Refresh Interval Time	7.8		µs	1
tQH	Output DQS Valid Window	tHP - tQHS		ns	5
tHP	Clock Half Period	tCL(min) or tCH(min)		ns	
tQHS	Data Hold Skew Factor		0.75	ns	
tWPST	DQS Write Postable Time	0.4	0.6	tCK	3
tRAP	Active to READ with Autoprecharge Command	20			
tDAL	Autoprecharge Write Recovery + Precharge Time	(tWR/tCK) + (tRP/tCK)		tCK	11

(AC Timing Parameters continued on next page.)

Notes:

- Maximum burst refresh of 8.
- The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to Logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- A write command can be applied with tRCD satisfied after this command.
- For registered DIMMs, tCL and tCH are $\approx 45\%$ of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
- Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate (V/ns)	Δt_{IS} (ps)	Δt_{IH} (ps)
0.5	0	0
0.4	50	50
0.3	100	100

This derating table is used to increase t_{IS} /t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

- I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate (V/ns)	Δt_{DS} (ps)	Δt_{DH} (ps)
0.5	0	0
0.4	75	75
0.3	150	150

This derating table is used to increase t_{DS} /t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

- I/O Setup/Hold Plateau Derating

I/O Input Level (mV)	Δt_{DS} (ps)	Δt_{DH} (ps)
± 280	50	50

This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below VREF \pm 310mV for a duration of up to 2ns.

- I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate (ns/V)	Δt_{DS} (ps)	Δt_{DH} (ps)
0	0	0
± 0.25	50	50
± 0.5	100	100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = - 0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

- This parameter is for system simulation purpose. It is guaranteed by design.

REVISION HISTORY

Rev. Change Description from Previous Revision

-101 02/28/2007. Initial release.

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