

128M x 64 Bit (1GB) 184-Pin DDR <1U Unbuffered DIMM (PC2100) 2 Ranks x 8; RoHS Compliant, Lead-Free

## FEATURES

- PC2100 Compliant (DDR266B 133MHz-7.5ns@CL-tRCD-tRP: 2.5-3-3)
- 184-Pin UDIMM form factor
- Auto and Self-Refresh capability (8,192 cycles/64ms refresh)
- SSTL\_2 compatible inputs and outputs
- 2.5V +/-0.1V VDD and VDDQ
- DDR2 architecture: Two data accesses per clock cycle, differential clock inputs (CK0, /CK0), bi-directional data strobe (DQS)
- Four internal component banks for concurrent operation
- Auto Precharge option for each burst access
- Data Mask (DM) for masking write data
- Burst Lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts
- RoHS Compliant Lead-Free

## GENERAL DESCRIPTION

The SL64C8M128M8L-B75EWU is a 128M x 64 bit (1GMB) 184-pin Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Unbuffered Dual In-line Memory Module (UDIMM).

The module consists of sixteen CMOS 16M x 8 bit x 4 bank DDR SDRAMs in lead-free 66-pin 400-mil TSOP-II packages mounted in 2 ranks on a 184-pin glass epoxy substrate.

A serial EEPROM using the two pin I<sup>2</sup>C protocol is also mounted to provide the Serial Presence Detects (SPD). Decoupling capacitors of 0.22µF are also mounted. Damping resistors are added for DQ, DQS, and DM signals.

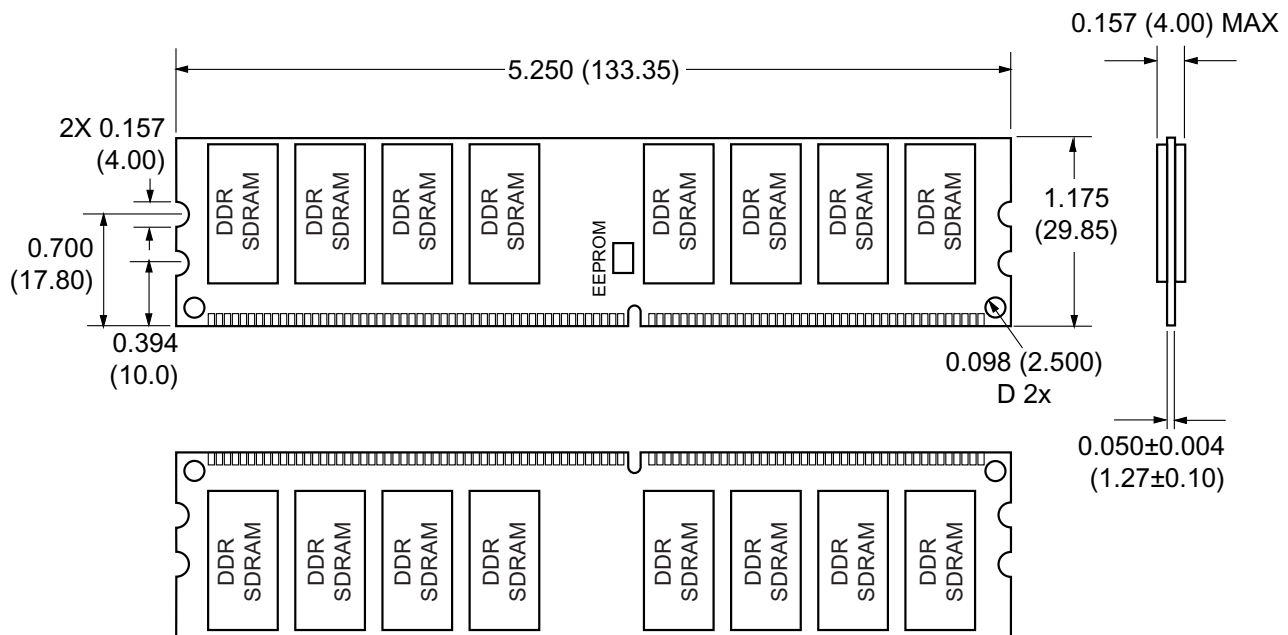
The module has gold edge connections and is intended for mounting into 184-pin UDIMM edge connector sockets keyed for 2.5V VDD and VDDQ.

## ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL64C8M128M8L-B75EWU	2.5	133	2.1 GB/s

## PACKAGE DIMENSIONS (Board No.: 1077)

Units are in inches (millimeters). All dimensions are typical unless otherwise specified.



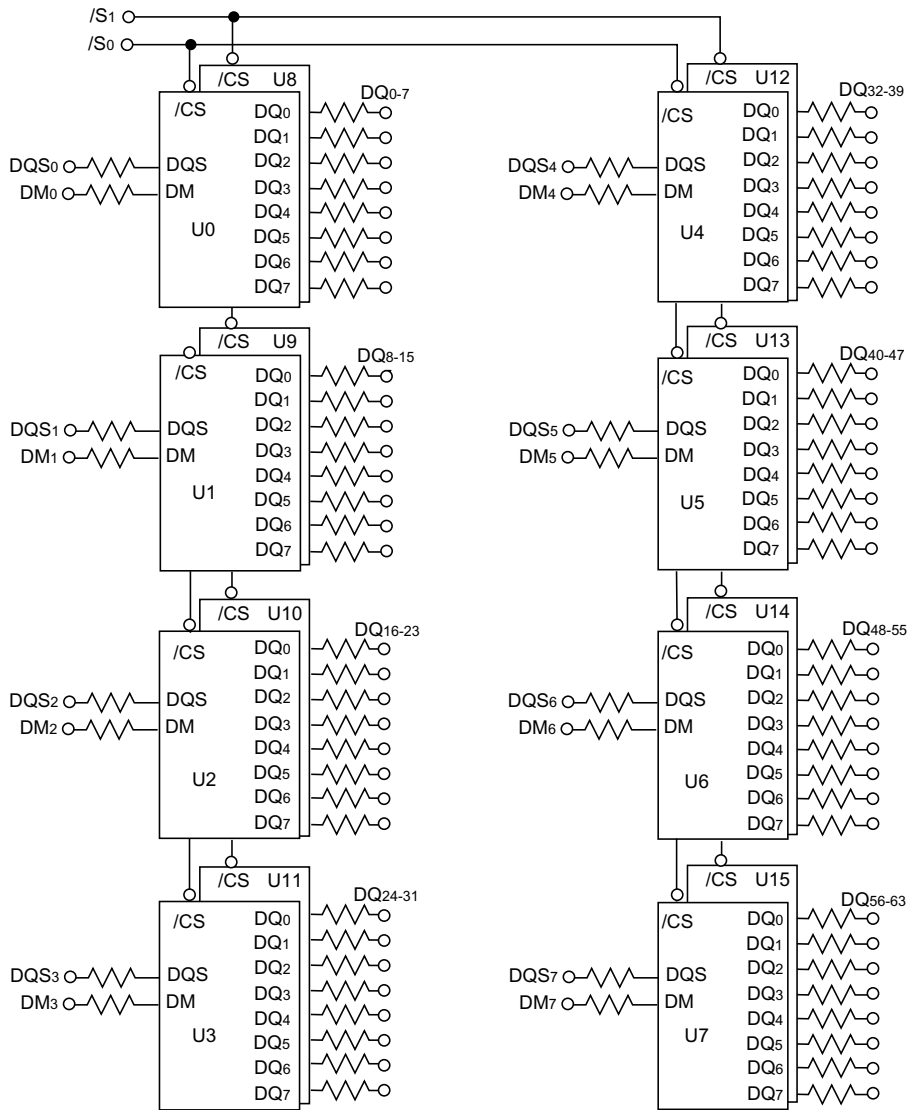
**PIN CONFIGURATION** (\* = Not Used; / = Active Low; **Bold Box** = Key)**184-PIN UDIMM PINOUT**

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	VSS	32	A5	124	VSS	62	VDDQ	154	/RAS
2	DQ0	94	DQ4	33	DQ24	125	A6	63	/WE	155	DQ45
3	VSS	95	DQ5	34	VSS	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	/CAS	157	/S0
5	DQS0	97	DM0	36	DQS3	128	VDDQ	66	VSS	158	/S1
6	DQ2	98	DQ6	37	A4	129	DM3	67	DQS5	159	DM5
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	VSS
8	DQ3	100	VSS	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	VSS	70	VDD	162	DQ47
10	/RESET*	102	NC	41	A2	133	DQ31	71	/S2*	163	/S3*
11	VSS	103	FETEN*	42	VSS	134	CB4	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	CB5	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	CB0	136	VDDQ	74	VSS	166	DQS3
14	DQS1	106	DQ13	45	CB1	137	CK0	75	CK2	167	A13*
15	VDDQ	107	DM1	46	VDD	138	/CK0	76	/CK2	168	VDD
16	CK1	108	VDD	47	DQS8*	139	VSS	77	VDDQ	169	DM6
17	/CK1	109	DQ14	48	A0	140	DM8*	78	DQS6	170	DQ54
18	VSS	110	DQ15	49	CB2	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1	50	VSS	142	CB6	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	CB3	143	VDDQ	81	VSS	173	NC
21	CKE0	113	BA2*	52	BA1	144	CB7	82	VDDID*	174	DQ60
22	VDDQ	114	DQ20	Key		Key		83	DQ56	175	DQ61
23	DQ16	115	A12	53	DQ32	145	VSS	84	DQ57	176	VSS
24	DQ17	116	VSS	54	VDDQ	146	DQ36	85	VDD	177	DM7
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	VSS	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DM2	57	DQ34	149	DM4	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	VSS	150	DQ38	89	VSS	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	VDDQ	122	A8	60	DQ35	152	VSS	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

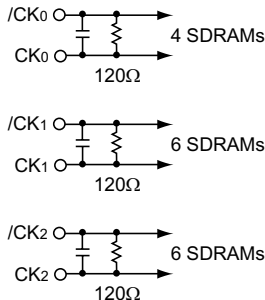
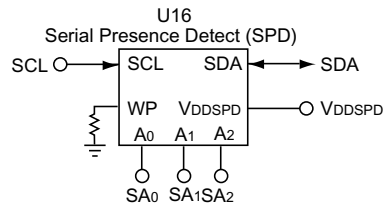
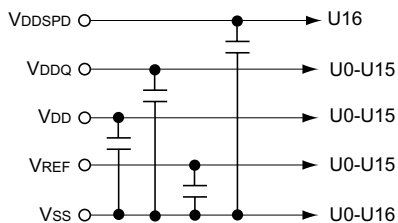
**PIN CONFIGURATION** (Continued) (\* = Not Used; / = Active Low)**PIN FUNCTIONS**

Symbol	Description
A0-A11, A12, A13*	SDRAM Address Bus
BA0-BA1, BA2*	SDRAM Bank Select
DQ0-DQ63	DIMM Memory Data Bus
CB0*-CB7*	DIMM ECC Check Bits
/RAS	SDRAM Row Address Strobe
/CAS	SDRAM Column Address Strobe
/WE	SDRAM Write Strobe
/S0, /S1, /S2*, /S3*	SDRAM Chip Select Lines (Physical Banks 0, 1, 2, and 3)
CKE0, CKE1	SDRAM Clock Enable Lines
DQS0-DQS7, DQS8*	SDRAM Data Strobes
DM0-DM7, DM8*	SDRAM Data Mask
VDDID*	VDD Identification Flag
CK0, CK1, CK2	SDRAM Clock (Positive Line, Differential Pair)
/CK0, /CK1, /CK2	SDRAM Clock (Negative Line, Differential Pair)
SCL	IIC Serial Bus Clock for EEPROM
SDA	IIC Serial Bus Data Line for EEPROM
SA0-SA2	IIC Slave Address Select for EEPROM
VDD	SDRAM Positive Power Supply
VDDQ	SDRAM I/O Driver Positive Power Supply
VREF	SDRAM I/O Reference Supply
VSS	Power Supply Return (Ground)
VDDSPD	Serial EEPROM Positive Power Supply (2.2V to 5.5V)
NC	Spare Pins (No Connect)
/RESET*	Reset Pin (Forces Register Inputs Low)
FETEN*	FET Enable Line

## FUNCTIONAL BLOCK DIAGRAM



- BA0-BA1 → BA0-BA1: SDRAMs U0-U15
- A0-A12 → A0-A12: SDRAMs U0-U15
- /RAS → /RAS: SDRAMs U0-U15
- /CAS → /CAS: SDRAMs U0-U15
- CKE0 → CKE0: SDRAMs U0-U7
- CKE1 → CKE1: SDRAMs U8-U15
- /WE → /WE: SDRAMs U0-U15



- NOTES:
1. DQ wiring may be changed within a byte.
  2. DQ, DQS, DM, CKE, /S relationships must be maintained as shown.
  3. DQ, DQS, and DM resistors are 22 ohms.

**SERIAL PRESENCE DETECT INFORMATION**

Serial PD Interface Protocol: I2C; Current sink capability of SDA driver  $\leq 3\text{mA}$ ; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
0	Number of SPD Bytes used by Manufacturer	128	80h
1	Total Number of Bytes in SPD Device	256	08h
2	Fundamental Memory Type	DDR SDRAM	07h
3	Number of Row Addresses on Assembly	13	0Dh
4	Number of Column Addresses on Assembly	11	0Bh
5	Number of Module Ranks	2	02h
6	Module Data Width	64	40h
7	Module Data Width (Continued)	-	00h
8	Module Voltage Interface Levels	SSTL 2.5V	04h
9	SDRAM Cycle Time, tCYC, CL = 2.5	7.5ns	75h
10	SDRAM Access from Clock, tAC, CL = 2.5	0.75ns	75h
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	7.8 $\mu$ s/SELF	82h
13	SDRAM Device Width (Primary SDRAM)	x8	08h
14	Error-checking SDRAM Data Width	None	00h
15	Min. CLK Delay for Back-to-Back Rand. Col. Addr., tCCD	1 CLK	01h
16	Burst Lengths Supported	2, 4, 8	0Eh
17	Number of Banks on SDRAM Device	4	04h
18	CAS Latencies Supported	2.0, 2.5	0Ch
19	CS Latencies Supported	0	01h
20	Write Latencies Supported	1	02h
21	SDRAM Module Attributes	Differential Clock	20h
22	SDRAM Device Attributes: General	VDD+/-0.2V	00h
23	Minimum Clock Cycle Time, tCYC, CL = 2	10ns	A0h
24	Max. Data Access Time from Clock, tAC, CL = 2	0.75ns	75h
25	Minimum Clock Cycle Time, tCYC, CL = 1.5	N/A	00h
26	Max. Data Access Time from Clock, tAC, CL = 1.5	N/A	00h
27	Minimum Row Precharge Time, tRP	20ns	50h
28	Minimum Row Active to Row Active, tRRD	15ns	3Ch
29	Minimum /RAS to /CAS Delay, tRCD	20ns	50h
30	Minimum /RAS Pulse Width, tRAS	45ns	2Dh
31	Module Rank Density	512MB	80h
32	Minimum Address and Command Setup Time, tAS	0.9ns	90h
33	Minimum Address and Command Hold Time, tAH	0.9ns	90h
34	Minimum Data/Data Mask Input Setup Time, tDS	0.5ns	50h
35	Minimum Data/Data Mask Input Hold Time, tDH	0.5ns	50h
36 - 40	Reserved	-	00h

(Serial Presence Detect Information continued on next page.)

**SERIAL PRESENCE DETECT INFORMATION** (continued)Serial PD Interface Protocol: I2C; Current sink capability of SDA driver  $\leq 3\text{mA}$ ; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
41	Row Cycle Time, tRC	65ns	41h
42	Auto Refresh Cycle Time, tRFC	75ns	48h
43	SDRAM Device Max. Cycle Time, tCKMAX	13ns	34h
44	SDRAM Device Max. DQS-DQ Skew Time, tDQSQ	0.50ns	32h
45	SDRAM Device Max. Read Data Hold Skew Factor, tQHS	0.75ns	75h
46	Reserved	-	00h
47	DDR SDRAM DIMM Height	1.125" 1.25" (1.175")	01h
48 - 61	Reserved	-	00h
62	SPD Revision	JEDEC 1.0	10h
63	Checksum for Bytes 0 - 62	JEDEC Calculation	xxh
64	Manufacturer's JEDEC ID Code per JEP-106E	Continuation Code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71	—	—	00h
72	Manufacturing Location	STEC USA	01h
73-90	Module Part Number (ASCII)	—	00h
91	Module Revision Code	Engineering (00) Rev. A (01) Rev. B (02)	01h
92	—	—	00h
93	Year of Manufacture (BCD)	Year (BCD)	yyh
94	Week of Manufacture (BCD)	Week (BCD)	wwh
95	Module Serial Number	Tester Number	ssh
96		Serial # (Bits 7-0)	ssh
97		Serial # (Bits 15-8)	ssh
98		Serial # (Bits 23-16)	ssh
99	Manufacturer-Specific Data (RSVD)	S	53h
100		T	54h
101		E	45h
102		C	43h
103-127	None	-	00h
128-255	Open for Customer Use	-	00h

## ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to higher than recommended voltages for extended periods may affect device reliability.

Symbol	Parameter	Value	Unit
VIN, VOUT	Voltage on any Pin Relative to VSS	-1.0 to +3.6	V
VDD	Voltage on VDD Supply Relative to VSS	-1.0 to +3.6	V
VDDQ	Voltage on VDDQ Supply Relative to VSS	-1.0 to +3.6	V
TSTG	Storage Temperature	-55 to +125	°C
PD	Power Dissipation	24	W
IOS	Short Circuit Current	50	mA

## POWER and DC OPERATING CONDITIONS (SSTL\_2 IN/OUT)

Recommended Operating Conditions (Voltage referenced to VSS = 0V. TA = 0 to 70°C).

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Supply Voltage (for device with a nominal VDD of 2.6V)	2.3	2.7	V	
VDDQ	I/O Supply Voltage	2.3	2.7	V	
VREF	I/O Reference Voltage	VDDQ/2-50mV	VDDQ/2+50mV	V	1
VTT	I/O Termination Voltage (System)	VREF-0.04	VREF+0.04	V	2
VIH(DC)	Input Logic High Voltage	VREF+0.15	VDDQ+0.3	V	4
VIL(DC)	Input Logic Low Voltage	-0.3	VREF-0.15	V	4
VIN(DC)	Input Voltage Level, CK and /CK	0.3	VDDQ+0.3	V	
VID(DC)	Input Differential Voltage, CK and /CK	0.3	VDDQ+0.6	V	3
IL	Input Leakage Current:  A, BA, /RAS, /CAS, /WE CKE, /S CK0, /CK0 CK1, /CK1 DM	-32	32	µA	
		-16	16	µA	
		-8	8	µA	
		-12	12	µA	
		-4	4	µA	
IOZ	Output Leakage Current:  DQ, CB, DQS	-10	10	µA	
IOH	Output High Current (VOUT = VTT+0.84V) (Normal Strength Driver)	-16.8		mA	
IOL	Output Low Current (VOUT = VTT-0.84V) (Normal Strength Driver)	16.8		mA	

### Notes:

- Includes  $\pm 25\text{mV}$  margin for DC offset on VREF, and a combined total of  $\pm 50\text{mV}$  margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in V REF noise. VREF should be de-coupled with an inductance of  $\leq 3\text{nH}$ .
- V TT is not applied directly to the device. V TT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
- VID is the magnitude of the difference between the input level on CK and the input level on /CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
- The value of VIX is expected to equal  $0.5 \cdot \text{VDDQ}$  of the transmitting device and must track variations in the dc level of the same.
- These characteristics obey the SSTL-2 class II standards.

## DC CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted. Module IDD was calculated on the basis of component IDD and can be measured differently according to DQ loading capacity. VDD = 2.7V. TA = 10°C.

Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; t RC = t RC (MIN); t CK = t CK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;	IDD0*	960	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; t RC = t RC (MIN); t CK = t CK (MIN); IOU = 0mA; Address and control inputs changing once per clock cycle	IDD1*	1,200	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t CK = t CK (MIN); CKE = (LOW)	IDD2P**	80	mA
IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; t CK = t CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F**	360	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t CK = t CK (MIN); CKE = LOW	IDD3P**	280	mA
ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; t RC = t RAS (MAX); t CK = t CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N**	400	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); IOU = 0mA	IDD4R*	1,200	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W*	1,120	mA
AUTO REFRESH CURRENT: t RC = t RC(MIN)	IDD5*	2,280	mA
SELF REFRESH CURRENT: CKE <= 0.2V	IDD6**	80	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, t RC = t RC (MIN); t CK = t CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7*	2,840	mA

\* In a module with more than one rank, IDDn is calculated with one rank in IDDn and the other ranks in IDD2P.

\*\* All ranks in IDDn.

where n = corresponding IDD condition listed in Symbol column.

and Values shown for DDR SDRAM components only

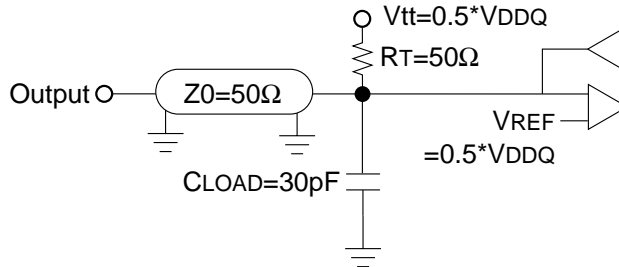
**AC OPERATING CONDITIONS**

Recommended Operating Conditions. VDD = VDDQ = 2.6V, TA = 25°C, f = 1MHz.

Symbol	Parameter/Condition	Min	Max	Units	Notes
VIH(AC)	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	VREF+0.31		V	3
VIL(AC)	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals		VREF-0.31	V	3
VID(AC)	Input Differential Voltage, CK and /CK Inputs	0.7	VDDQ+0.6	V	1
VIX(AC)	Input Crossing Point Voltage, CK and /CK Inputs	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

**Notes:**

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of V IX is expected to equal 0.5\*V DDQ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relation to a Vref envelope that has been bandwidth limited 20MHz.



Output Load Circuit (SSTL\_2)

**CAPACITANCE**

VDD = VDDQ = 2.6V, TA = 25°C, f = 1MHz.

Symbol	Parameter	Max	Units
CIN0	Input Capacitance: A, BA, /RAS, /CAS, /WE, CKE, /S (30pF added for board)	78	pF
CIN1	Input Capacitance: CKE, /S (30pF added for board)	54	pF
CIN2	Input Capacitance: CK0, /CK0 (10pF added for board)	22	pF
CIN3	Input Capacitance: CK1, /CK1 (10pF added for board)	28	pF
CI/O	Data, DQS I/O, DM Input Capacitance: DQ, DQS, DM (5pF added for board)	15	pF

(AC Operating Conditions continued on next page.)

**AC TIMING PARAMETERS** (These AC Characteristics were tested on the component.)

Symbol	Parameter	Min	Max	Unit	Notes
tRC	Row Cycle Time	65		ns	
tRFC	Refresh Row Cycle Time	75		ns	
tRAS	Row Active Time	45	120K	ns	
tRCD	/RAS to /CAS Delay	20		ns	
tRP	Row Precharge Time	20		ns	
tRRD	Row Active to Row Active Delay	15		ns	
tWR	Write Recovery Time	15		ns	
tWTR	Internal Write to Read Command Delay	1		tCK	
tCK	Clock Cycle Time	CL=3.0 CL=2.5 CL=2	N/A 12 12	ns	
tCH	Clock High Level Width	0.45	0.55	tCK	4
tCL	Clock Low Level Width	0.45	0.55	tCK	4
tDQSK	DQS-Out Access Time from CK, /CK	-0.75	0.75	ns	
tAC	Output Data Access Time from CK, /CK	-0.50	0.75	ns	
tDQSQ	Data Strobe Edge to Output Data Edge		0.5	ns	
tRPRE	Read Preamble	0.9	1.1	tCK	
tRPST	Read Postamble	0.4	0.6	tCK	
tDQSS	CK to Valid DQS-In	0.75	1.25	tCK	
tWPRES	DQS-In Setup Time	0		ns	2
tWPRE	Write Preamble	0.25		tCK	
tDSS	DQS Falling Edge to CK Rising-Setup Time	0.2		tCK	
tDSH	DQS Falling Edge from CK Rising-Hold Time	0.2		tCK	
tDQSH	DQS-In High Level Width	0.35		tCK	
tDQSL	DQS-In Low Level Width	0.35		tCK	
tIS	Address and Control Input Setup Time	0.9		ns	5
tIH	Address and Control Input Hold Time	0.9		ns	5
tHZ	Data-Out High Impedence Time from CK,/CK	-0.75	0.75	ns	
tLZ	Data-Out Low Impedence Time from CK,/CK	0.75	0.75	ns	
tMRD	Mode Register Set Cycle Time	2		ns	
tDS	DQ and DM Setup Time to DQS	0.5		ns	6, 7, 8
tDH	DQ and DM Hold Time to DQS	0.5		ns	6, 7, 8
tDIPW	DQ and DM Input Pulse Width	1.75		ns	
tIPW	Control and Address Input Pulse Width for Each Input	2.2		ns	
tXSNR	Exit Self-Refresh to any Non-Read Command	75		ns	
tXSRD	Exit Self-Refresh to any Read Command	200		tCK	
tREFI	Refresh Interval Time		7.8	μs	1
tQH	Output DQS Valid Window	tHPmin -tQHS		ns	
tHP	Clock Half Period	tCLmin or tCHmin		ns	
tQHS	Data Hold Skew Factor		0.75	ns	
tWPST	DQS Write Postamble Time	0.4	0.6	tCK	3
tRAP	Active to Autoprecharge Delay	15		ns	
N/A	Data Valid Output Window	tQH - tDQSQ		ns	9

## Notes:

1. The refresh period is 64ms. This equates to an average refresh rate of 7.8125μs. However, an AUTO REFRESH command must be asserted at least once every 70.3μs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High\_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. For registered DIMMs, tCL and tCH are ≥ 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.

### 5. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase tIS /tIH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

### 6. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase tDS /tDH in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

### 7. I/O Setup/Hold Plateau Derating

I/O Input Level	ΔtDS	ΔtDH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

### 8. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

9. The valid data window is derived by achieving other specifications: tHP (tCK/2), tDQSQ, and tQH (tQH = tHP - tQHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain.

## REVISION HISTORY

### Rev. Change Description from Previous Revision

-101 04/27/2007. Initial release.

## DISCLAIMER OF LIABILITY

STEC™ Inc. reserves the right to make changes to specifications and product descriptions such as but not limited to numbers, parameters and other technical information contained herein without notice. Please contact the STEC™ Inc. sales office to obtain the latest specifications. STEC™ Inc. grants no warranty with respect to this datasheet, neither explicit or implied, and is not liable for direct or indirect damages. Some states do not grant the exclusion of incidental damages and as such this statement may not be valid in such states. The provisions of the datasheet do not convey to the purchaser of the device any license under any patent rights or other intellectual property rights of STEC Inc. or others.

## EXPORT ADMINISTRATION REGULATIONS

The information provided may be subject to United States Export Controls. Such information should not be downloaded or exported (i), into (or to a national or resident of) Cuba, Iraq, Libya, North Korea, Iran, Syria, or any other country to which the United States has embargoed goods; or given to (ii), anyone on the United States Treasury Department's list of Specially Designated Nationals or the U.S. Commerce Department's Table of Deny Orders. By using the information, you represent and warrant that you are not located in, under the control of, or a national or resident of any such country or on any such list.

## COPYRIGHT NOTICE

Copyright © 2007 by STEC™ Inc. All rights reserved. Information contained in this document, including but not limited to any instructions, descriptions and product specifications, is considered proprietary and confidential to STEC™, Inc. and shall not be modified, used, copied, reproduced or disclosed in whole or in part, in any form or by any means, electronic or mechanical, for any purpose, without the written consent of STEC™ Inc.

