

128M x 64 Bit (1GB) 240-Pin DDR3 Unbuffered DIMM (PC3-8500) 1 Rank x 8  
RoHS Compliant and Halogen-Free

## GENERAL DESCRIPTION

The SL64Y8W128M8L-A18JTG is a 128M x 64 bit (1GB) 240-pin Double Data Rate 3 (DDR3) Unbuffered Dual In-line Memory Module (UDIMM).

The module consists of eight CMOS 16M x 8 bit x 8 bank DDR3 SDRAMs in lead-free BGA packages mounted in 1 rank on a 240-pin glass epoxy substrate.

A serial EEPROM using the two pin I<sup>2</sup>C protocol is also mounted to provide the Serial Presence Detects (SPD). Decoupling capacitors are mounted across the power supply. Damping resistors are added in series for DQ, DQS, and DM signals.

The module has gold edge connections and is intended for mounting into 240-pin UDIMM edge connector sockets keyed for 1.5V.

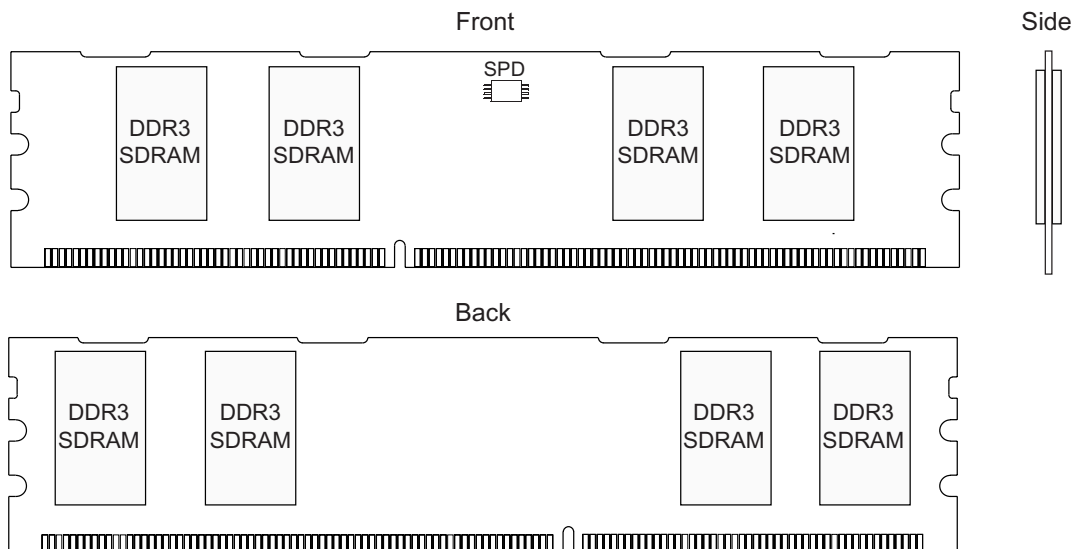
## FEATURES

- PC3-8500 Compliant (DDR3-1066 533MHz-1.875ns@CL-tRCD-tRP: 7-7-7)
- 240-Pin UDIMM form factor
- Average Periodic Refresh Interval (tREFI)
  - 7.8125µs Max for 0°C < T<sub>OPR</sub> < 85°C (64ms/8,196 cycles)
  - 3.9µs Max for 85°C < T<sub>OPR</sub> < 95°C (32ms/8,196 cycles)
- V<sub>DD</sub> = V<sub>DDQ</sub> = 1.5V ± 0.075V
- JEDEC Standard 1.5V I/O (SSTL\_15 compatible)
- V<sub>DDSPD</sub> = 1.425V to 1.575V
- DDR3 Architecture: Two data accesses per clock cycle, differential clock inputs (CK, /CK), differential data strobe (DQS, /DQS), Off-Chip Driver (OCD) Impedance Adjustment, Dynamic On Die Termination (ODT), On Chip Delay Locked Loop (DLL); Eight-bit prefetch architecture
- Commands entered on each rising CK edge; DQS-edge aligned with data for READs and center-aligned with data for WRITES; DLL to align DQ and DQS transitions with CK
- Eight internal component banks for concurrent operation
- Asynchronous RESET Pin Support
- ZQ Calibration Support
- Concurrent Auto Precharge option is supported
- Data Mask (DM) for Masking Write Data
- Programmable Burst Lengths: 4 (Burst Chop), 8 (Nibble Sequential and Interleave Mode)
- /CAS READ Latency (CL): 6, 7, 8
- /CAS WRITE Latency (CWL): 5, 6 - tCK
- Posted /CAS Additive Latency (AL): 0, CL - 1, CL - 2
- Adjustable Data-Output Drive Strength
- Serial Presence Detect (SPD) with EEPROM
- Gold Edge Contacts
- RoHS Compliant and Halogen-Free

## ORDERING INFORMATION

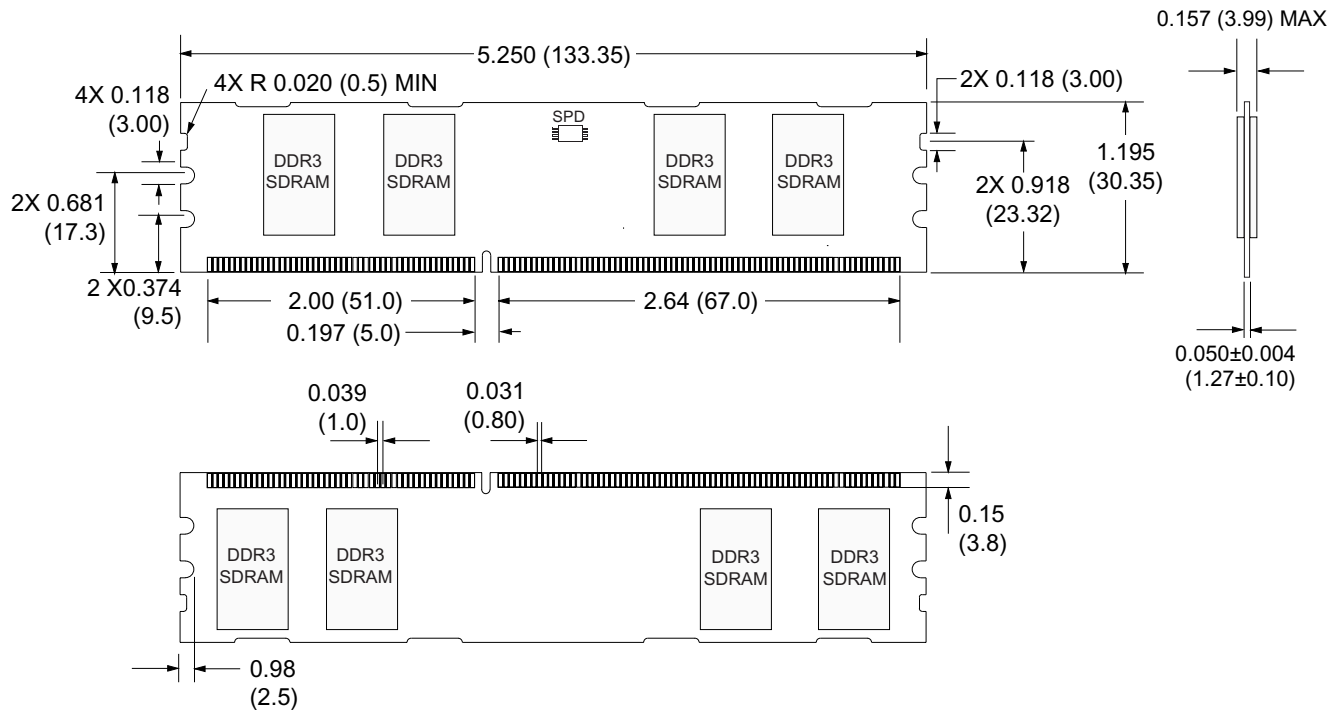
Part Number	Module Speed	DRAM Speed	CL-tRCD-tRP
SL64Y8W128M8L-A18JTG	PC3-8500	DDR3-1066	7-7-7

## 240-PIN UDIMM ILLUSTRATION



## PACKAGE DIMENSIONS (Board No.: 1701)

Units are in inches (millimeters). All dimensions are typical unless otherwise specified.



**PIN CONFIGURATION** (\* = Not Used; / = Active Low; **Bold Line** = Key)

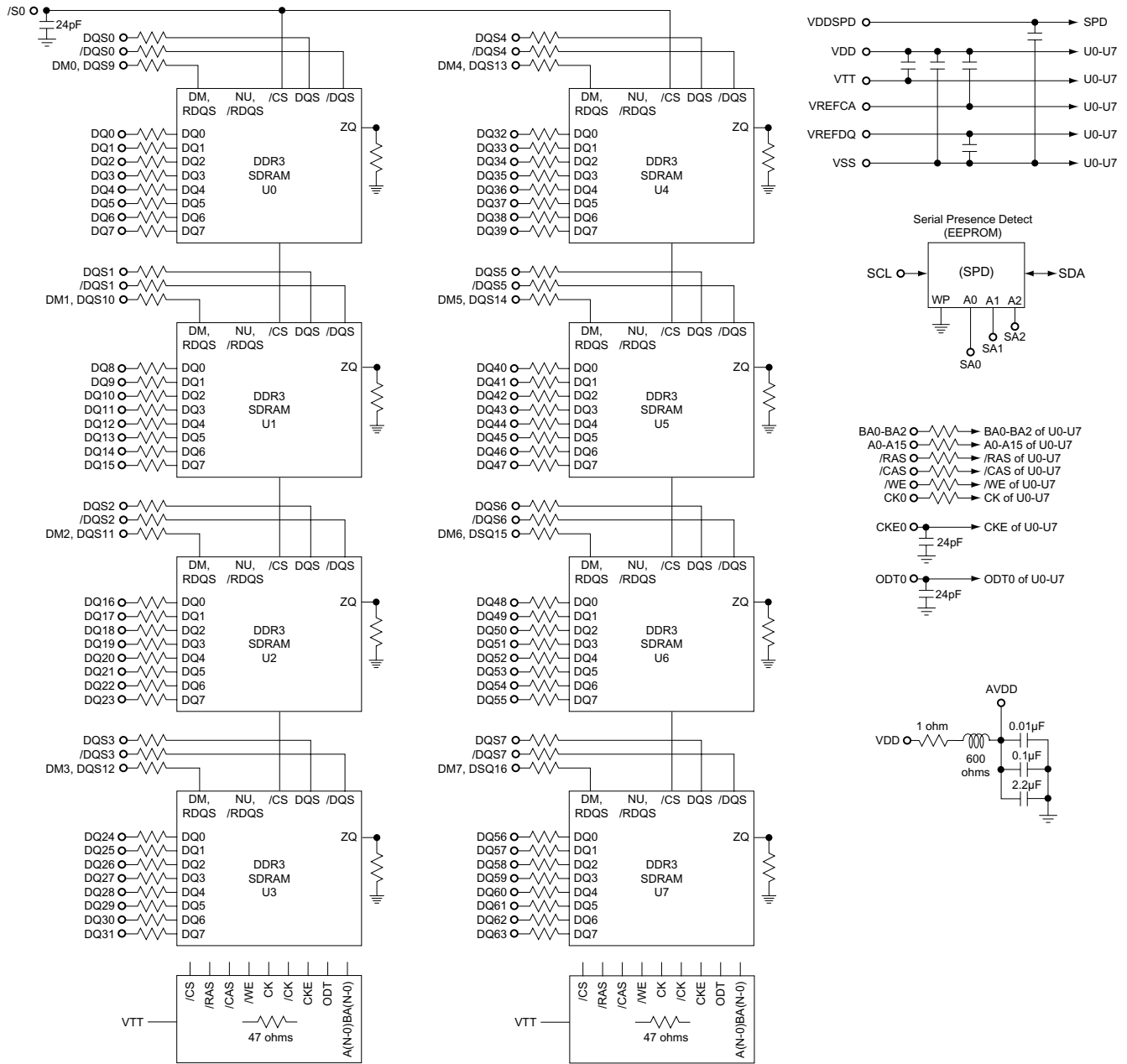
**240-PIN UDIMM PINOUT**

240-Pin UDIMM Front Pinout						240-Pin UDIMM Back Pinout									
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3, DQS12	182	VDD	212	DM5, DQS14
3	DQ0	33	/DQS3	63	CK1*	93	/DQS5	123	DQ5	153	/DQS12	183	VDD	213	/DQS14
4	DQ1	34	DQS3	64	/CK1*	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0, DQS9	155	DQ30	185	/CK0	215	DQ46
6	/DQS0	36	DQ26	66	VDD	96	DQ42	126	NC, /DQS9	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	/EVENT*	217	VSS
8	VSS	38	VSS	68	PAR_IN*	98	VSS	128	DQ6	158	CB4*	188	A0	218	DQ52
9	DQ2	39	CB0*	69	VDD	99	DQ48	129	DQ7	159	CB5*	189	VDD	219	DQ53
10	DQ3	40	CB1*	70	A10	100	DQ49	130	VSS	160	VSS	190	BA1/BA0	220	VSS
11	VSS	41	VSS	71	BA0/BA1	101	VSS	131	DQ12	161	DM8, DQS17	191	VDD	221	DM6, DQS15
12	DQ8	42	/DQS8*	72	VDD	102	/DQS6	132	DQ13	162	NC, /DQS17	192	/RAS	222	/DQS15
13	DQ9	43	DQS8*	73	/WE	103	DQS6	133	VSS	163	VSS	193	/S0	223	VSS
14	VSS	44	VSS	74	/CAS	104	VSS	134	DM1, DQS10	164	CB6*	194	VDD	224	DQ54
15	/DQS1	45	CB2*	75	VDD	105	DQ50	135	NC, /DQS10	165	CB7*	195	ODT0	225	DQ55
16	DQS1	46	CB3*	76	/S1	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1	107	VSS	137	DQ14	167	NC (TEST)	197	VDD	227	DQ60
18	DQ10	48	VTT*	78	VDD	108	DQ56	138	DQ15	168	/RESET	198	/S3*	228	DQ61
19	DQ11	49	VTT*	79	RFU/SPD	109	DQ57	139	VSS	169	CKE1	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7, DQS16
21	DQ16	51	VDD	81	DQ32	111	/DQS7	141	DQ21	171	A15	201	DQ37	231	/DQS16
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	/ERR_OUT*	83	VSS	113	VSS	143	DQS11	173	VDD	203	DM4, DQS13	233	DQ62
24	/DQS2	54	VDD	84	/DQS4	114	DQ58	144	/DQS11	174	A12	204	/DQS13	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	VSS	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

**PIN CONFIGURATION** (Continued) (\* = Not Used; / = Active Low)**PIN FUNCTIONS**

Symbol	Type	Description
CK0	Input	Clock Input, Positive Line
/CK0	Input	Clock Input, Negative Line
CKE0, CKE1	Input	Clock Enable
/RAS	Input	Row Address Strobe
/CAS	Input	Column Address Strobe
/WE	Input	Write Enable
/S0, /S1*, /S2*, /S3*	Input	Chip Select
ODT0, ODT1*	Input	On Die Termination
DM0-DM8	Input	Data Masks
DQS0-DQS17	Input/Output	Data Strobes
/DQS0-/DQS17	Input/Output	Data Strobes, Negative Line
BA0-BA2	Input	Bank Address Inputs
A0-A9, A11, A13-A15	Input	Address Inputs
A10 /AP	Input	Address Input/Autoprecharge
A12 /BC	Input	Address Input/Burst Chop
DQ0-DQ63	Input/Output	Data Input/Output
CB0-CB7*	Input/Output	Data Check Bits
SCL	Input	Serial Clock for Presence Detect
SA0-SA2	Input	Presence Detect Address Inputs
SDA	Input/Output	Serial Presence Detect Data
/RESET	Input	Register and SDRAM Control
NC		No Connect
RFU		Reserved for Future Use
/EVENT		Reserved for Optional Hardware Temperature Testing
TEST		Memory Bus Test Tool (NC and not used for DIMMs)
VDDSPD	Supply	Serial EEPROM Positive Power Supply: 1.7V to +3.6V
VDD	Supply	Power Supply: 1.8V±0.1V
VSS	Supply	Ground
VREFDQ	Supply	Reference Voltage for DQ
VREFCA	Supply	Reference Voltage for CA
PAR_IN*	Input	Parity Bit for the Address and Command Bus ("1": Odd, "0": Even)
ERR_OUT*	Output	Parity Error Found in the Address or Command Bus

## FUNCTIONAL BLOCK DIAGRAM



**Notes:**

1. ZQ resistors are 240 Ohms +/-1% unless otherwise noted.
2. DQ to I/O wiring may be changed within a byte.
3. If a Thermal Sensor is not included in the alternate SPD, then a separate SPD and TS are required.
4. Unused register inputs ODT1 and CKE1 have a 330 ohm resistor to ground.
5. /S2, /S3, CKE1, ODT1, CK1 and /CK1 are not connected.

**SERIAL PRESENCE DETECT INFORMATION**

Serial PD Interface Protocol:  $\dot{P}C$ ; Current sink capability of SDA driver  $\leq 3mA$ ; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
0	Number of Serial Presence Detect Bytes Written/ SPD Device Size/CRC Coverage	Size = 256 CRC = 116 Bytes Used = 176	92h
1	SPD Revision	Revision 1.0	10h
2	Key Byte/DRAM Device Type	DDR3 SDRAM	0Bh
3	Key Byte/Module Type	UDIMM Width = 133.35mm Nom	02h
4	SDRAM Density and Banks	1Gb Density 8 Internal Banks	02h
5	SDRAM Device Row and Column Count	13 Rows 10 Columns	09h
6	Reserved	-	00h
7	Module Organization	1 Rank x8 Device Width	01h
8	Module Memory Bus Width	Non-ECC 64-Bit Primary Bus Width	03h
9	Fine Timebase (FTB) Dividend/Divisor (Pico Seconds)	5/2 = 2.5ps	52h
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)	01h
11	Medium Timebase (MTM) Divisor	1/8 (0.125ns)	08h
12	SDRAM Minimum Cycle Time, tCK(min)	1.875ns	0Fh
13	Reserved	-	00h
14	CAS Latencies Supported, Least Significant Byte (LSB)	Low Byte CL Supported = 6, 7, 8	1Ch
15	CAS Latencies Supported, Most Significant Byte (MSB)	High Byte CL Supported = 00h	00h
16	CAS Latency Time, tAA(min)	13.125ns	69h
17	Write Recovery Time, tWR(min)	15ns	78h
18	/RAS to /CAS Delay, tRCD(min)	13.125ns	69h
19	Minimum Row Active to Row Active Delay Time, tRRD(min)	7.5ns	3Ch
20	Minimum Row Precharge Delay Time, tRP(min)	13.125ns	69h
21	tRAS and tRC Upper Nibbles	- -	11h
22	Minimum Active to Precharge Delay Time, tRAS(min), LSB	37.5ns	2Ch
23	Minimum Active to Active/Refresh Delay Time, tRC(min), LSB	50.625ns	95h
24	Minimum Refresh Recovery Delay Time, tRFC(min), LSB	110ns	70h
25	Minimum Refresh Recovery Time, tRFC(min), MSB	110ns	03h
26	Minimum Internal Write to Read Command Delay Time, tWTR(min)	7.5ns	3Ch
27	Minimum Internal Read to Precharge Command Delay Time, tRTP(min)	7.5ns	3Ch
28	Upper Nibble for tFAW	-	01h
29	Minimum Four Active Window Delay, LSB, tFAW(min)	40ns	40h
30	SDRAM Optional Features	DLL-Off Mode Support RZQ/6 Support	81h
31	SDRAM Thermal and Refresh Options	ODTS, ASR, Ext. Temp. Range	0Dh
32	Module Thermal Sensor	1 = Thermal Sensor	01h
33	Module Thermal Heat Spreader Solution	0 = No Heat Spreader	00h
34	SDRAM Device Type	0 = Standard Monolithic	00h
35 - 59	-	-	00h

(Serial Presence Detect Information continued on next page.)

**SERIAL PRESENCE DETECT INFORMATION** (continued)Serial PD Interface Protocol: I<sup>2</sup>C; Current sink capability of SDA driver <=3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
60	Module Nominal Height	30 < Height <= 31mm	10h
61	Module Maximum Thickness	Back: 1 < Thickness <= 2mm Front: 1 < Thickness <= 2mm	11h
62	Reference Raw Card Used	Raw Card A, Rev D	00h
63	Address Mapping, 1st Rank, Edge Connector to DRAM	Standard	00h
64 - 116	Reserved	-	xxh
117	Module Manufacturer's JEDEC ID Code	STEC	01h
118			A8h
119	Module ID: Module Manufacturing Location	USA (01h)/Malaysia (02h)	01h/02h
120	Module ID: Module Manufacturing Date		00h
121			00h
122	Module ID: Module Serial Number		00h
123			00h
124			00h
125			00h
126	Cyclical Redundancy Code		56h
127			54h
128	Module Part Number	6	36h
129		4	34h
130		Y	59h
131		8	38h
132		W	57h
133		1	31h
134		2	32h
135		8	38h
136		M	4Dh
137		8	38h
138		L	4Ch
139		-	2Dh
140		A	41h
141		1	31h
142		8	38h
143		J	4Ah
144		T	54h
145	G	47h	
146	Module Revision Code		00h
147			00h
148	DRAM Manufacturer's JEDEC ID Code	JEP-106	xxh
149			xxh
150-175	Manufacturer's Specific Data		00h
176-255	Open for Customer Use		00h

## ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to higher than recommended voltages for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Units
VDD	VDD Supply Voltage relative to VSS	-0.4	1.975	V
VDDQ	VDDQ Supply Voltage relative to VSS	-0.4	1.975	V
VIN, VOUT	Voltage on any Pin relative to VSS	-0.4	1.975	V
TSTG	Storage Temperature	-55	+100	°C
TOPR	Operating Temperature-DRAM Components			
	Commerical Operating Temperature	0	85	°C
TA	Industrial Operating Temperature	TBD	TBD	°C
	Operating Temperature-Module, Ambient			
	Commerical Operating Temperature	0	85	°C
	Industrial Operating Temperature	TBD	TBD	°C

### Notes:

- Case temperature, TOPR, is the case surface temperature on the center/top side of the DRAM. Please refer to the JESD51.2 standard for the measurement conditions.
- Case temperature range between 0°C to 85°C is the range which all DRAM specifications are supported.
- For case temperature ranges between 85°C to 95°C, a doubling of the refresh commands in frequency to a 32ms period ( $t_{REFI} = 3.9\mu s$ ) is required. To enter self-refresh mode at this temperature range, an EMRS command is required to change the internal refresh rate.

## RECOMMENDED DC OPERATING CONDITIONS

All voltages referenced to VSS.

Symbol	Parameter	Min	Nom	Max	Units	Notes
VDD	Supply Voltage	1.425	1.5	1.575	V	1
VDDQ	I/O Supply Voltage	1.425	1.5	1.575	V	4
VREF	I/O Reference Voltage	$0.49 \times VDDQ$	$0.50 \times VDDQ$	$0.51 \times VDDQ$	V	2
VTT	I/O Termination Voltage (System)	$VDDQ/2 - TBD$	VREF	$VDDQ/2 + TBD$	mV	3

### Notes:

- VDD and VDDQ must track each other. VDDQ must be less than or equal to VDD.
- VREF is expected to equal  $VDDQ/2$  of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed  $\pm 1$  percent of the DC value. Peak-to-peak AC noise on VREF may not exceed  $\pm 2$  percent of VREF (DC). This measurement is to be taken at the nearest VREF bypass capacitor.
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
- VDDQ tracks with VDD; VDDL tracks with VDD.

**INPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS****INPUT DC LOGIC LEVELS**

Symbol	Parameter	Min	Max	Units	Notes
V <sub>IH</sub> (DC)	Input High (Logic 1) Voltage	V <sub>REF</sub> + 100	TBD	mV	1
V <sub>IL</sub> (DC)	Input Low (Logic 0) Voltage	-TBD	V <sub>REF</sub> - 100	mV	1
V <sub>REFDQ</sub> (DC)	I/O Reference Voltage (DQ)	0.49*V <sub>DDQ</sub>	0.51*V <sub>DDQ</sub>	V	2, 3
V <sub>REFCA</sub> (DC)	I/O Reference Voltage (CMD/ADD)	0.49*V <sub>DDQ</sub>	0.51*V <sub>DDQ</sub>	V	2, 3
V <sub>TT</sub>	Termination Voltage	V <sub>DDQ</sub> /2 - TBD	V <sub>DDQ</sub> /2 + TBD	V	2, 3

**INPUT AC LOGIC LEVELS**

Symbol	Parameter	Min	Max	Units	Notes
V <sub>IH</sub> (AC)	Input High (Logic 1) Voltage	V <sub>REF</sub> + 175	-	mV	1, 2
V <sub>IL</sub> (AC)	Input Low (Logic 0) Voltage	-	V <sub>REF</sub> - 175	mV	1, 2

**DIFFERENTIAL INPUT LOGIC LEVELS**

Symbol	Parameter	Min	Max	Units	Notes
V <sub>IHdiff</sub>	Differential Input High Logic	+200	-	mV	
V <sub>ILdiff</sub>	Differential Input Low Logic	-	-200	mV	
V <sub>Ix</sub>	Differential Cross-Point Voltage relative to V <sub>DD</sub> /2	-150	150	mV	

**Notes:**

1. For DQ and DM, V<sub>REF</sub> = V<sub>REFDQ</sub>. For input only pins except RESET, or V<sub>REF</sub> = V<sub>REFCA</sub>.
2. The AC peak noise on V<sub>REF</sub> may not allow V<sub>REF</sub> to deviate from V<sub>REF</sub>(DC) by more than +/-1% V<sub>DD</sub> (approximately +/-15mV for reference).
3. Approximately V<sub>DD</sub>/2 +/-15mV.

## OUTPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

### AC OUTPUT LEVELS

Symbol	Parameter	Value	Units	Notes
VOH(AC)	AC Output High Measurement Level (SR Output)	$V_{TT} + 0.1 \times V_{DDQ}$	V	1
VOL(AC)	AC Output Low Measurement Level (SR Output)	$V_{TT} - 0.1 \times V_{DDQ}$	V	1

### DC OUTPUT LEVELS

Symbol	Parameter	Value	Units	Notes
VOH(DC)	DC Output High Measurement Level (IV Curve Linearity)	$0.8 \times V_{DDQ}$	V	
VOM(DC)	DC Output Mid Measurement Level (IV Curve Linearity)	$0.5 \times V_{DDQ}$	V	
VOL(DC)	DC Output Low Measurement Level (IV Curve Linearity)	$0.2 \times V_{DDQ}$	V	

### DIFFERENTIAL AC and DC OUTPUT PARAMETERS

Symbol	Parameter	Value	Units	Notes
VOHdiff(AC)	AC Differential Output High Measurement Level (SR Output)	$+0.2 \times V_{DDQ}$	V	2
VOLdiff(DC)	AC Differential Output Low Measurement Level (SR Output)	$-0.2 \times V_{DDQ}$	V	2

#### Notes:

1. The swing of  $\pm 0.1 \times V_{DDQ}$  is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 ohms and an effective test load of 25 ohms to  $V_{TT} = V_{DDQ}/2$ .
2. The swing of  $\pm 0.2 \times V_{DDQ}$  is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 ohms and an effective test load of 25 ohms to  $V_{TT} = V_{DDQ}/2$  at each of the differential outputs.

**IDD SPECIFICATIONS AND CONDITIONS**

IDD specifications are tested after the device is properly initialized. Recommended Operating Conditions. VDD = +1.5V ±0.075V, VDDQ = +1.5V ±0.075V, VDDL = +1.5V ±0.075V, VREF = VDDQ/2.

Input slew rate is specified by AC Parametric Test Conditions. IDD parameters are specified with ODT disabled. Data bus consists of DQ, DQS, and /DQS. IDD values must be met with all combinations of EMR bits 10 and 11.

Definitions for IDD Conditions:

- LOW is defined as VIN ≤ VIL (AC) (MAX)
- HIGH is defined as VIN ≥ VIH (AC) (MIN)
- STABLE is defined as inputs stable at a HIGH or LOW level
- FLOATING is defined as inputs at VREF = VDDQ/2
- SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
- Switching is defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes

**GENERAL IDD PARAMETERS**

IDD Parameter	DDR3-1066	Units
tCKmin(IDD)	1.875	ns
CL(IDD)	7	tCK
tRCDmin(IDD)	13.13	ns
tRCmin(IDD)	50.63	ns
tRASmin(IDD)	37.5	ns
tRPmin(IDD)	13.13	ns
tFAW(IDD)	x4/x8	37.5
	x16	N/A
tRRD(IDD)	x4/x8	10
	x16	N/A
tRFC(IDD) - 512Mb	N/A	ns
tRFC(IDD) - 1Gb	110	ns
tRFC(IDD) - 2Gb	N/A	ns
tRFC(IDD) - 4Gb	N/A	ns

**IDD7 CONDITIONS**

IDD7: Operating Current, specifies detailed timing requirements for IDD7. Changes will be required if timing parameter changes are made to the specification.

**IDD7 OPERATING CURRENT**

All Bank Interleave Read operation; legend: **A** = Active; **RA** = Read Auto Precharge; **D** = Deselect

All device banks are being interleaved at minimum tRC (IDD) without violating tRRD (IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOOUT = 0mA.

IDD7 Timing Parameters
A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D
A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D

## DDR3 IDD SPECIFICATIONS AND CONDITIONS

Symbol	Parameter/Condition
<b>IDD0</b>	<b>Operating One Bank Active-Precharge Current</b>
	tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
<b>IDD1</b>	<b>Operating One Bank Active-Read-Precharge Current</b>
	IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.
<b>IDD2P<sub>(0)</sub></b>	<b>Precharge Power-Down Current (Slow Exit)</b>
	All device banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING. Slow Exit – MR0 A12 Bit = 0.
<b>IDD2P<sub>(1)</sub></b>	<b>Precharge Power-Down Current (Fast Exit)</b>
	All device banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING. Fast Exit – MR0 A12 Bit = 1.
<b>IDD2Q</b>	<b>Precharge Quiet Standby Current</b>
	All device banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.
<b>IDD2N</b>	<b>Precharge Standby Current</b>
	All device banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
<b>IDD3P</b>	<b>Active Power-Down Current</b>
	All device banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.
<b>IDD3N</b>	<b>Active Standby Current</b>
	All device banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
<b>IDD4W</b>	<b>Operating Burst Write Current</b>
	All device banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
<b>IDD4R</b>	<b>Operating Burst Read Current</b>
	All device banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.
<b>IDD5B</b>	<b>Burst Refresh Current</b>
	tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
<b>IDD6</b>	<b>Self Refresh Current</b>
	CK and /CK at 0V; CKE <= 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.
<b>IDD6ET</b>	<b>Extended Temperature Range Self-Refresh Current</b>
	CK and /CK at 0V; CKE <= 0.2V; Other control and address bus inputs are FLOATING, PASR disabled. Applicable for MR2 setting A6 = 0 and A7 = 1.
<b>IDD6TC</b>	<b>Auto Self-Refresh Current</b>
	CK and /CK at 0V; CKE <= 0.2V; Other control and address inputs are FLOATING, PASR disabled. Applicable for MR2 setting A6 = 1 and A7 = 0.
<b>IDD7</b>	<b>Operating Bank Interleave Read Current</b>
	All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.

## MAXIMUM DDR3 IDD VALUES

Symbol	DDR3-1066	Units
IDD0	880	mA
IDD1	1,000	mA
IDD2P <sub>1</sub>	80	mA
IDD2P <sub>2</sub>	104	mA
IDD2N	520	mA
IDD2Q	480	mA
IDD3P	320	mA
IDD3N	600	mA
IDD4W	1,440	mA
IDD4R	1,600	mA
IDD5	N/A	mA
IDD5 <sub>B</sub>	2,520	mA
IDD6	80	mA
IDD6 <sub>L</sub>	N/A	mA
IDD6 <sub>ET</sub>	N/A	mA
IDD6 <sub>TC</sub>	N/A	mA
IDD7	3,510	mA

## Notes:

- For IDD0, IDD1, IDD4W, IDD5 and IDD7:

In a module with more than one rank, IDD<sub>n</sub> is calculated with one rank in the IDD<sub>n</sub> and the other ranks in IDD2N.

For IDD2P, IDD2Q, IDD2N, IDD3P, IDD3N and IDD6:

where *n* = corresponding IDD condition listed in the Symbol column.

- Values shown for DDR3 SDRAM components only.
- Values will differ according to the DRAM parts used to manufacture the module.
- IDD values are calculated using worst-case specifications of currently available DRAMs from different manufacturers.
- For Industrial Operating Temperature Range:

When T<sub>CASE</sub> ≤ 0°C:

- IDD2P and IDD3P (Slow) must be derated by 4 percent
- IDD4R and IDD5W must be derated by 2 percent
- IDD6 and IDD7 must be derated by 7 percent

When T<sub>CASE</sub> ≤ 85°C:

- IDD0, IDD1, IDD2N, IDD2Q, IDD3N, IDD3P (Fast), IDD4R, IDD4W and IDD5W must be derated by 2 percent
- IDD2P must be derated by 20 percent
- IDD3P (Slow) must be derated by 30 percent
- IDD6 must be derated by 80 percent (IDD6 will increase by this amount if T<sub>CASE</sub> < 85°C and the 2x refresh option is still enabled)

## CAPACITANCE

VDD = +1.5V ±0.075V, VDDQ = +1.5V ±0.075V, VREF = VSS, *f* = 100 MHz, Recommended Operating Temperature Range, VOUT (DC) = VDDQ/2, VOUT (Peak-to-Peak) = 0.1V; DM input is grouped with I/O pins because DM and the I/O pins are matched in loading.

TBD

**SPEED BINS - DDR3-1066**

Recommended Operating Temperature Range; VDDQ = VDD = 1.5V +/-0.075V

Speed Bins	Symbol	Minimum	Maximum	Units
Internal READ Command to First Data	tAA	13.125	20	ns
ACT to Internal READ or WRITE Delay Time	tRCD	13.125	-	ns
PRE Command Period	tRP	13.125	-	ns
ACT to ACT or REF Command Period	tRC	50.625	-	ns
ACT to PRE Command Period	tRAS	37.5	9*tREFI	ns
CL = 5	CWL = 5 tCK(avg)	Reserved		ns
	CWL = 6 tCK(avg)	Reserved		ns
CL = 6	CWL = 5 tCK(avg)	2.5	3.3	ns
	CWL = 6 tCK(avg)	Reserved		ns
CL = 7	CWL = 5 tCK(avg)	Reserved		ns
	CWL = 6 tCK(avg)	1.875	< 2.5	ns
CL = 8	CWL = 5 tCK(avg)	Reserved		ns
	CWL = 6 tCK(avg)	1.875	< 2.5	ns
Supported CL Settings		6, 7, 8		nCK
Supported CWL Settings		5, 6		nCK

**SPEED BIN NOTES:**

1. The CL and CWL settings result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When selecting a tCK(AVG), both need to be fulfilled.
2. tCK(AVG).MIN limits. CAS Latency is not strictly analog; the data and strobe output are synchronized by the DLL. All possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5 or 1.25 nanoseconds) when calculating CL [nCK] = tAA [ns], rounding up to the next 'supported CL'.
3. tCK(AVG).MAX limits: tCK(AVG) = tAA.MAX/CLSELECTED, rounding the tCK(AVG) down to the next valid speed bin limit (3.3ns or 2.5ns, or 1.875ns or 1.25ns). This result is tCK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. The user must program a different value.
5. 'Optional' settings allow certain devices to support this setting, but it is not a mandatory feature. Refer to the datasheet of the supplier and SPD information to determine if and how this setting is supported.
6. Any DDR3 speed bin also supports functional operation at lower frequencies as indicated in the table but are verified by design only and not production tests.
7. tREFI is dependent on operating temperature (TOPR).

**CLOCK JITTER AND TIMING PARAMETERS**

Recommended Operating Temperature Range; VDDQ = VDD = 1.5V +/-0.075V

<b>Input Clock Jitter</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Maximum</b>	<b>Units</b>
Average Clock Period	tCK(avg)	1,875	3,333	ps
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps
<b>Clock</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Maximum</b>	<b>Units</b>
Minimum Clock Cycle Time (DLL Off Mode)	tCK(DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	See Speed Bins Table		ps
Clock Period	tCK(abs)	tCK(avg) Min + tJIT(per) Min	tCK(avg) Max + tJIT(per) Max	ps
Clock Period Jitter	tJIT(per)	-90	90	ps
Clock Period Jitter during DLL Locking Period	tJIT(per_tck)	-80	80	ps
Cycle to Cycle Period Jitter	tJIT(cc)	180		ps
Cycle to Cycle Period Jitter during DLL Locking Period	tJIT(cc_tck)	160		ps
Cumulative Jitter Error, 2 Cycles	tERR(2per)	TBD	TBD	ps
Cumulative Jitter Error, 3 Cycles	tERR(3per)	TBD	TBD	ps
Cumulative Jitter Error, 4 Cycles	tERR(4per)	TBD	TBD	ps
Cumulative Jitter Error, 5 Cycles	tERR(5per)	TBD	TBD	ps
Cumulative Error across $n = 6, 7, 8, 9, 10$ Cycles	tERR(6-10per)	TBD	TBD	ps
Cumulative Error across $n = 11, 12...49, 50$ Cycles	tERR(11-50per)	TBD	TBD	ps
Average High Pulse Width	tCH(avg)	0.47	0.53	tCK(avg)
Average Low Pulse Width	tCH(avg)	0.47	0.53	tCK(avg)
Duty Cycle Jitter	tJIT(duty)	-75	75	ps
<b>Data</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Maximum</b>	<b>Units</b>
DQS, /DQS to DQ Skew, per Group, per Access	tDQSQ	-	150	ps
DQ Output Hold Time from DQS, /DQS	tQH	0.36	-	tCK(avg)
DQ Low-Impedance Time from CK, /CK	tLZ(DQ)	-600	300	ps
DQ High-Impedance Time from CK, /CK	tHZ(DQ)	-	300	ps
Data Setup Time to DQS, /DQS referenced to VIH(AC) VIL(AC) Levels	tDS(base)	25	-	ps
Data Hold Time to DQS, /DQS referenced to VIH(AC) VIL(AC) Levels	tDH(base)	100	-	ps
DQ and DM Input Pulse Width for each Input	tDIPW	0.35	-	tCK(avg)
<b>Data Strobe</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Maximum</b>	<b>Units</b>
DQS, /DQS READ Preamble	tRPRE	0.9	-	tCK
DQS, /DQS Differential READ Postamble	tRPST	0.3	-	tCK
DQS, /DQS Output High Time	tQSH	0.38	-	tCK(avg)
DQS, /DQS Output Low Time	tQSL	0.38	-	tCK(avg)
DQS, /DQS WRITE Preamble	tWPRE	0.9	1.1	tCK
DQS, /DQS WRITE Postamble	tWPST	0.4	0.6	tCK
DQS, /DQS Rising Edge Output Access Time from Rising CK, /CK	tDQCK	-265	265	ps
DQS, /DQS Low-Impedance Time (Referenced from RL-1)	tLZ(DQS)	-600	300	ps
DQS, /DQS High-Impedance Time (Referenced from RL+BL/2)	tHZ(DQS)	-	300	ps
DQS, /DQS Differential Input Low Pulse Width	tDQSL	0.4	0.6	tCK
DQS, /DQS Differential Input High Pulse Width	tDQSH	0.4	0.6	tCK
DQS, /DQS Rising Edge to CK, /CK Rising Edge	tDQSS	-0.25	0.25	tCK(avg)
DQS, /DQS Falling Edge Setup Time to CK, /CK Rising Edge	tDSS	0.2	-	tCK(avg)
DQS, /DQS FALLING Edge Hold Time to CK, /CK Rising Edge	tDSH	0.2	-	tCK(avg)

(Timing Parameters continued on next page.)

**TIMING PARAMETERS** (continued)

Recommended Operating Temperature Range; VDDQ = VDD = 1.5V +/-0.075V

Command and Address	Symbol	Minimum	Maximum	Units
DLL Locking Time	tDLLK	512	-	nCK
Internal READ Command to PRECHARGE Command Delay	tRTP	Max (4tCK, 7.5ns)	-	
Delay from Start of Internal WRITE Transaction to Internal READ Command	tWTR	Max (4tCK, 7.5ns)	-	
WRITE Recovery Time	tWR	15	-	ns
Mode Register Set Command Cycle Time	tMRD	4		tCK(avg)
Mode Register Set Command Update Delay	tMOD	Max (12tCK, 15ns)	-	
ACTIVE to PRECHARGE Command Period	tRAS	37.5	70,000	ns
ACTIVE to ACTIVE Command Period, 1KB Page Size	tRRD	Max (4tCK, 7.5ns)	-	
ACTIVE to ACTIVE Command Period, 2KB Page Size	tRRD	Max (4tCK, 10ns)	-	
Four Activate Window, 1KB Page Size	tFAW	37.5	-	ns
Four Activate Window, 2KB Page Size	tFAW	50	-	ns
Command and Address Setup Time to CK, /CK referenced to VIH(AC)/VL(AC) Levels	tIS(base)	125	-	ps
Command and Address Hold Time to CK, /CK referenced to VIH(AC)/VL(AC) Levels	tIH(base)	200	-	ps
Control and Address Input Pulse Width for each Input	tIPW	0.6	-	tCK(avg)
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
Refresh	Symbol	Minimum	Maximum	Units
512Mb REFRESH/REFRESH or to ACTIVE Command Interval	tRFC	90	-	ns
1Gb REFRESH/REFRESH or to ACTIVE Command Interval	tRFC	110	-	ns
2Gb REFRESH/REFRESH or to ACTIVE Command Interval	tRFC	160	-	ns
4Gb REFRESH/REFRESH or to ACTIVE Command Interval	tRFC	300	-	ns
8Gb REFRESH/REFRESH or to ACTIVE Command Interval	tRFC	350	-	ns
Average Periodic Refresh Interval (0° <= TCASE <= 85°C)	tREFI		7.8	µs
Average Periodic Refresh Interval (85° <= TCASE <= 95°C)	tREFI		3.9	µs
Calibration	Symbol	Minimum	Maximum	Units
Power-Up and RESET Calibration Time	tZQinitl	512	-	tCK
Normal Operation Full Calibration Time	tZQoper	256	-	tCK
Normal Operation Short Calibration Time	tZQCS	64	-	tCK
Reset	Symbol	Minimum	Maximum	Units
Exit Reset from CK HIGH to a Valid Command	tXPR	Max(5tCK, tRFC + 10ns)	-	
Self-Refresh	Symbol	Minimum	Maximum	Units
Exit Self-Refresh to Commands not requiring a Locked DLL	tXS	Max(5tCK, tRFC + 10ns)	-	
Exit Self-Refresh to Commands requiring a Locked DLL	tXSDLL	tDLLK(min)	-	tCK
Minimum CK Low Width for Self-Refresh Entry to Exit Timing	tCKESR	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self-Refresh Entry, SRE	tCKSRE	Max(5tCK, 10ns)	-	
Valid Clock Requirement before Self-Refresh Entry, SRE	tCKSRX	Max(5tCK, 10ns)	-	

(Timing Parameters continued on next page.)

**TIMING PARAMETERS** (continued)

Recommended Operating Temperature Range; VDDQ = VDD = 1.5V +/-0.075V

<b>Power Down</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Maximum</b>	<b>Units</b>
Exit Power Down with DLL ON to any Valid Command; Exit Precharge Power Down with DLL frozen to commands that do not require a locked DLL	tXP	Max (3tCK, 7.5ns)	-	
Exit Precharge Power Down with DLL frozen to commands that do require a locked DLL	tXPDLL	Max (10tCK, 24ns)	-	
CKE Minimum Pulse Width	tCKE	Max 3(tCK, 5.625ns)	-	
Command Pass Disable Delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Timing of ACT Command to Power Down Entry	tACTPDEN	1	-	nCK
Timing of PRE Command to Power Down Entry	tPRPDEN	1	-	nCK
Timing of RD/RDA Command to Power Down Entry	tRDPDEN	RL + 4 + 1	-	
Timing of WR Command to Power Down Entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 + (tWR/tCK)	-	nCK
Timing of WRA Command to Power Down Entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 + WR + 1	-	nCK
Timing of WR Command to Power Down Entry (BL4MRS)	tWRPDEN	WL + 2 + (tWR/tCK)	-	nCK
Timing of WRA Command to Power Down Entry (BL4MRS)	tWRAPDEN	WL + 2 + WR + 1	-	nCK
Timing of REF Command to Power Down Entry	tREFPDEN	1	-	
Timing of MRS Command to Power Down Entry	tMRSDEN	tMOD(min)	-	tCK
<b>ODT</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Maximum</b>	<b>Units</b>
ODT High Time without WRITE Command or with WRITE Command and BC4	ODTH4	4	-	nCK
ODT High Time with WRITE Command and BL8	ODTH8	6	-	nCK
Asynchronous RTT Turn-On Delay (Power-Down with DLL Frozen)	tAONPD	1	9	ns
Asynchronous RTT Turn-Off Delay (Power-Down with DLL Frozen)	tAOFPD	1	9	ns
ODT Turn-On	tAON	-300	300	ps
RTT_NOM and RTT_WR Turn-Off Time from ODTLoff Reference	tAOF	0.3	0.7	tCK(avg)
RTT Dynamic Change Skew	tADC	0.3	0.7	tCK(avg)
<b>Write Leveling</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Maximum</b>	<b>Units</b>
First DQS Pulse Rising Edge after tDQSS Margining Mode is programmed	tWLMRD	40	-	tCK
DQS/DQS Delay after tDQS Margining Mode is programmed	tWLDQSEN	25	-	tCK
tDQSS Latch Setup Time	tWLS	0.15	-	tCK(avg)
tDQSS Latch Hold Time	tWLH	0.15	-	tCK(avg)
Write Leveling Output Delay	tWLO	0	9	ns
Write Leveling Output Error	tWLOE	0	2	ns

(Timing Parameters continued on next page.)

**CLOCK JITTER NOTES:**

1. The unit, 'tCK(avg)', represents the actual tCK(avg) of the input clock under operation; 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
2. These parameters are measured from a command/address signal (CKE, /CS, /RAS, /CAS, /WE ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal crossing. The specific values are not affected by the amount of clock jitter applied. The setup and hold are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present or absent.
3. These parameters are measured from a data strobe signal crossing to its respective clock signal crossing. The specific values are not affected by the amount of clock jitter applied. The setup and hold are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present or absent.
4. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc) transition edge to its respective data strobe signal (DQS(L/U)/DQS(L/U) crossing..
5. The DDR3 SDRAM device supports tnPARM [nCK] =  $RU\{tP\text{ARM} [ns] / tCK(avg)\}$ , which is in clock cycles, with the assumption that all input clock jitter specifications are satisfied.
6. The parameters are specified per their average values; however, the relationship between the average timing and the absolute instantaneous timing holds at all times.

**TIMING PARAMETER NOTES:**

1. Actual values are dependent on measurement level definitions. TBD.
2. READ (and RAP) and synchronous ODT commands require a locked DLL.
3. The maximum values are dependent on the system.
4. WR as programmed in the mode register.
5. RTT Turn-On Time (tAON) TBD.
6. RTT Turn-Off Time (tAOF) TBD.
7. tWR is in nanoseconds. To calculate tWRPDEN, tWR/tCK must be rounded up to the next integer.
8. WR is in clock cycles as programmed in MR0.
9. The maximum postamble is bound by tHZDQS(max).
10. Output timing deratings are relative to the SDRAM input clock. When the device operates with input clock jitter, the parameters need to be derated by TBD.
11. The TBD value is only valid for RON34.
12. TBD is a single-ended signal parameter.
13. tREFI is dependent on TOPR.
14. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, /CK differential slew rate. For DQ and DM signals, VREF(DC) = VRefDQ(DC). For input pins except RESET, VRef(DC) = VRefCA(DC).
15. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, /DQS differential slew rate. For DQ and DM signals, VREF(DC) = VRefDQ(DC). For input pins except RESET, VRef(DC) = VRefCA(DC).
16. The start of the internal write transaction is as follows:
  - For BL8 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
  - For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
  - For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
17. CKE is allowed to register LOW while operations such as row activation, precharge, autoprecharge, autoprecharge or refresh rate are in progress; however, the power-down IDD specification is not applied until such operations are completed.
18. CKE is allowed to register LOW after a REFRESH command once tREFPDEN(min) is satisfied; however, there are situations where additional time such as tXPDLL(min) is also required.
19.  $tJIT(duty) = +/-\{0.07 * tCK(avg) - [p.5 - (\min(tCH(avg), tCL(avg))) * tCK(avg)]\}$ . For example, if tCH/tCL was 0.48/0.52, tJIT duty would calculate out to +/- 125ps. The values listed for tCH(avg) and tCL(avg) must not be exceeded.

## REVISION HISTORY

### Rev. Change Description from Previous Revision

- 101 06/18/2007. Initial release.
- 102 09/18/2007. Updated functional block diagram, SPD and timing parameters to latest specification.
- 103 05/05/2009. P/N updated to Halogen-Free. IDD's calculated.

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