256M x 72 Bit (2GB) 240-Pin DDR3 Unbuffered DIMM (PC3-10600) 2 Ranks x 8
RoHS-6 Compliant and Halogen-Free

GENERAL DESCRIPTION

The SL72Y8W256M8M-A15LTG is a 256M x 72 bit (2GB) 240-pin Double Data Rate 3 (DDR3) Unbuffered Dual In-Line Memory Module (UDIMM) with data ECC.

The module consists of eighteen CMOS 16M x 8 bit x 8 bank DDR3 SDRAMs in lead-free BGA packages mounted in 2 ranks on a 240-pin glass epoxy substrate.

A serial EEPROM using the two pin I^2C protocol is also mounted to provide the Serial Presence Detects (SPD).

Decoupling capacitors are mounted across the power supply. Damping resistors are added in series for DQ, DQS and DM signals.

The module has gold edge connections and is intended for mounting into 240-pin UDIMM edge connector sockets keyed for 1.5V.

FEATURES

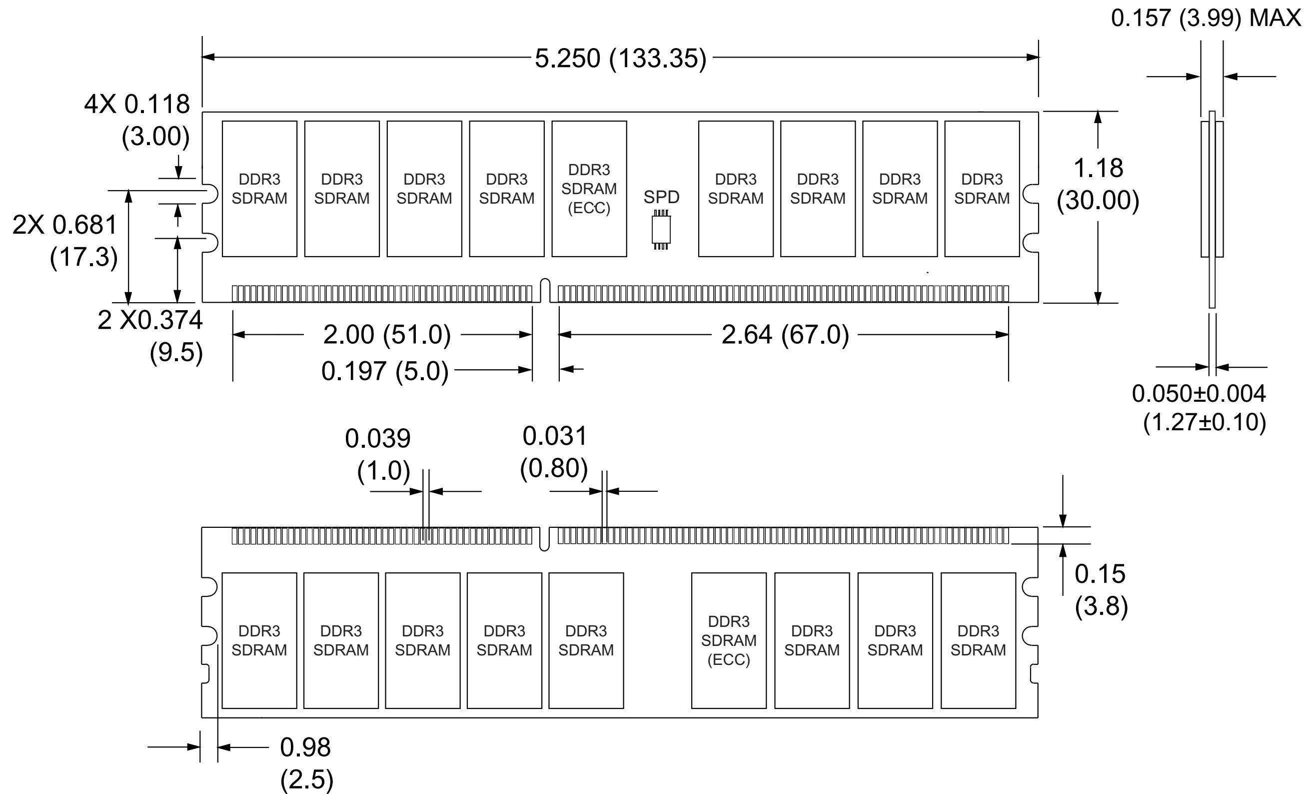
- PC3-10600 Compliant
  (DDR3-1333 667MHz-1.5ns@CL-^{t}RCD-^{t}RP: 9-9-9)
- 240-Pin UDIMM form factor
- Average Periodic Refresh Interval (^{t}REFI)
  - 7.8125ms Max for $0^oC < T_C < 85^oC$
    (64ms/8,196 cycles)
  - 3.9ms Max for $85^oC < T_C < 95^oC$
    (32ms/8,196 cycles)
- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- $V_{DDSPD} = 3.3V \pm 0.3V$
- JEDEC Standard 1.5V I/O (SSTL_15 compatible)
- DDR3 Architecture: Two data accesses per clock cycle, differential clock inputs (CK, /CK), bidirectional differential data strobe (DQS, /DQS), Off-Chip Driver (OCD), Impedance Adjustment, Dynamic On-Die Termination (ODT), On-Chip Delay Locked Loop (DLL); Eight-bit prefetch architecture
- Commands entered on each rising CK edge; DQS-edge aligned with data for READs and center-aligned with data for WRITEs; DLL to align DQ and DQS transitions with CK
- Eight internal component banks for concurrent operation
- Asynchronous RESET Pin Support
- ZQ Calibration Support
- Concurrent Auto Precharge option is supported
- Data Mask (DM) for masking Write data
- Programmable Burst Lengths: 4 (Burst Chop) and 8 (Nibble Sequential and Interleave Mode)
- /CAS READ Latency (CL): 6, 7, 8, 9, 10
- /CAS WRITE Latency (CWL): 5, 6, 7 -^{t}CK
- Posted /CAS Additive Latency (AL): 0, CL-1, CL-2
- Adjustable Data-Output drive strength
- Serial Presence Detect (SPD)
- ECC, 1-bit error detection and correction
- Gold edge contacts
- RoHS-6 Compliant and Halogen Free

ORDERING INFORMATION

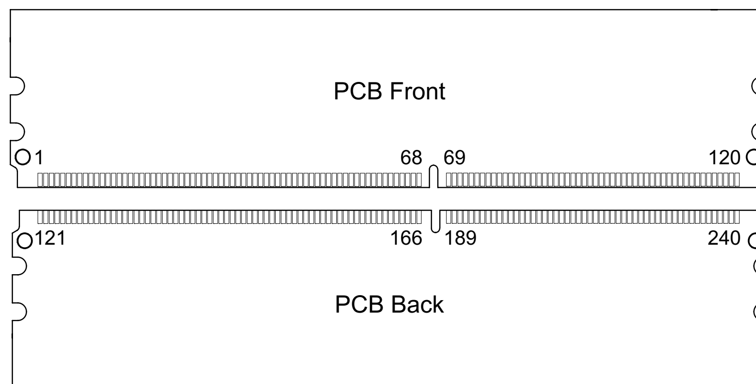
Part Number	Module Speed	DRAM Speed	CL-^{t}RCD-^{t}RP
SL72Y8W256M8M-A15LTG	PC3-10600	DDR3-1333	9-9-9

PACKAGE DIMENSIONS *(Board No. 1719)*

Units are in inches (millimeters). All dimensions are typical unless otherwise noted.



PIN LOCATIONS



PIN CONFIGURATION *(* = Not Used; / = Active Low; **Bold Line or Box** = **Key**)*

240-PIN UDIMM PINOUT

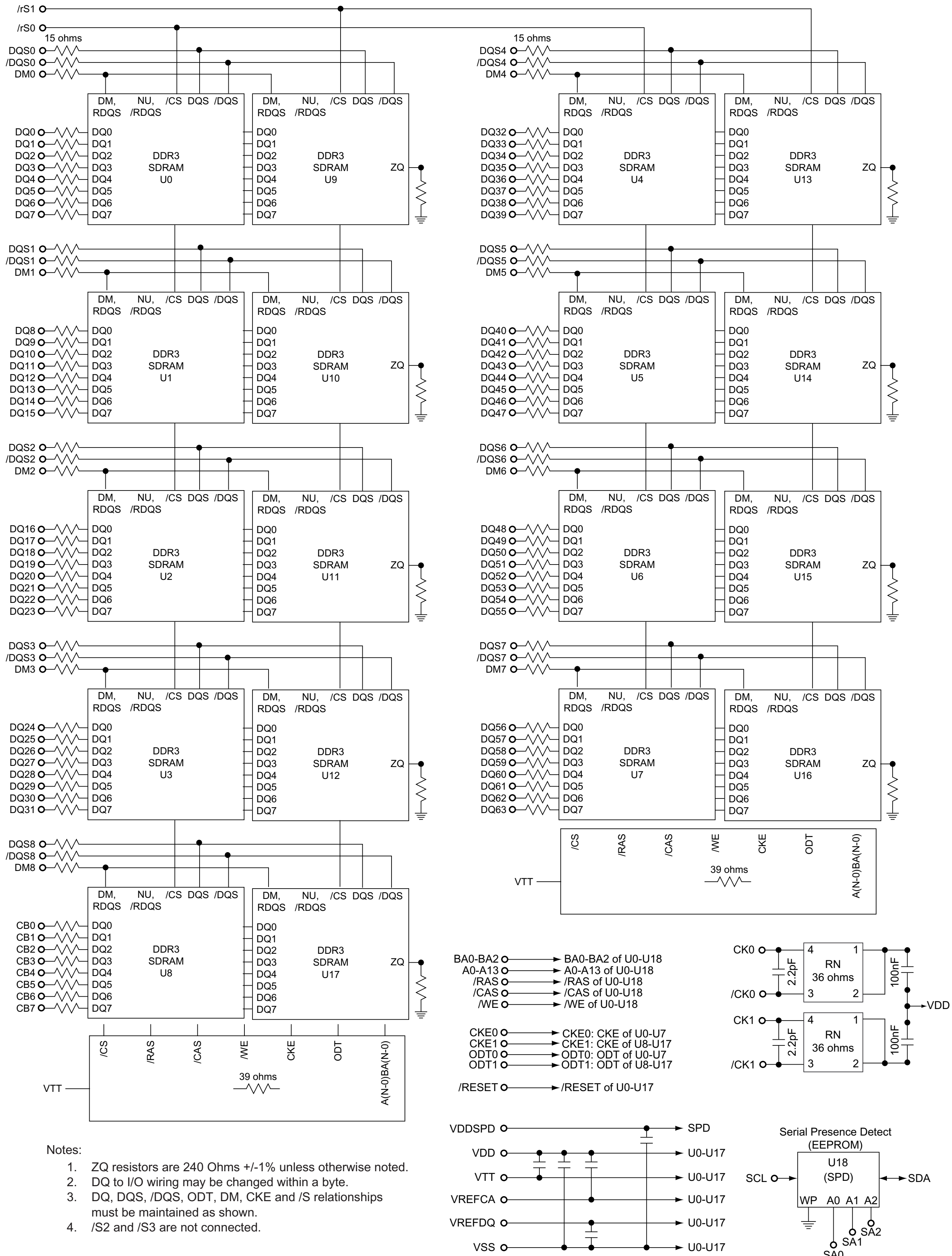
240-Pin UDIMM Front Pinout								240-Pin UDIMM Back Pinout							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3	182	VDD	212	DM5
3	DQ0	33	/DQS3	63	CK1	93	/DQS5	123	DQ5	153	NC	183	VDD	213	NC,
4	DQ1	34	DQS3	64	/CK1	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0,	155	DQ30	185	/CK0	215	DQ46
6	/DQS0	36	DQ26	66	VDD	96	DQ42	126	NC	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	/EVENT*	217	VSS
8	VSS	38	VSS	68	PAR_IN*	98	VSS	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10/AP	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	DM8	191	VDD	221	DM6
12	DQ8	42	/DQS8	72	VDD	102	/DQS6	132	DQ13	162	NC	192	/RAS	222	NC
13	DQ9	43	DQS8	73	/WE	103	DQS6	133	VSS	163	VSS	193	/S0	223	VSS
14	VSS	44	VSS	74	/CAS	104	VSS	134	DM1	164	CB6	194	VDD	224	DQ54
15	/DQS1	45	CB2	75	VDD	105	DQ50	135	NC	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	/S1	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1	107	VSS	137	DQ14	167	NC (TEST*)	197	VDD	227	DQ60
18	DQ10	48	NC (VTT)	78	VDD	108	DQ56	138	DQ15	168	/RESET	198	/S3*, NC	228	DQ61
19	DQ11	49	NC (VTT)	79	/S2	109	DQ57	139	VSS	169	CKE1	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7
21	DQ16	51	VDD	81	DQ32	111	/DQS7	141	DQ21	171	A15*	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14*	202	VSS	232	VSS
23	VSS	53	/ERR_OUT*	83	VSS	113	VSS	143	DM2	173	VDD	203	DM4	233	DQ62
24	/DQS2	54	VDD	84	/DQS4	114	DQ58	144	NC	174	A12, /BC	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

PIN CONFIGURATION *(Continued) (* = Not Used; / = Active Low)*

PIN FUNCTIONS

Symbol	Type	Description
CK0, CK1	Input	Clock Input, Positive Line
/CK0, /CK1	Input	Clock Input, Negative Line
CKE0, CKE1	Input	Clock Enable
/RAS	Input	Row Address Strobe
/CAS	Input	Column Address Strobe
/WE	Input	Write Enable
/S0, /S1, /S2*, /S3*	Input	Chip Select
ODT0, ODT1	Input	On Die Termination
DM0-DM8	Input	Data Masks
DQS0-DQS8	Input/Output	Data Strobes
/DQS0-/DQS8	Input/Output	Data Strobes, Negative Line
BA0-BA2	Input	Bank Address Inputs
A0-A9, A11, A13, A14*-A15*	Input	Address Inputs
A10 /AP	Input	Address Input/Autoprecharge
A12 /BC	Input	Address Input/Burst Chop
DQ0-DQ63	Input/Output	Data Input/Output
CB0-CB7	Input/Output	Data Check Bits
SCL	Input	Serial Clock for Presence Detect
SA0-SA2	Input	Presence Detect Address Inputs
SDA	Input/Output	Serial Presence Detect Data
/RESET	Input	SDRAM Reset Control
NC		No Connect
RFU		Reserved for Future Use
/EVENT*		Reserved for Optional Hardware Temperature Testing
TEST*		Memory Bus Test Tool (NC and not used for DIMMs)
VDDSPD	Supply	Serial EEPROM Positive Power Supply: 3.3V ±0.3V
VDD	Supply	Power Supply: 1.5V ±0.075V
VSS	Supply	Ground
VREFDQ	Supply	Reference Voltage for DQ
VREFCA	Supply	Reference Voltage for CA
PAR_IN*	Input	Parity Bit for the Address and Command Bus (“1”: Odd, “0”: Even)
ERR_OUT*	Output	Parity Error Found in the Address or Command Bus

FUNCTIONAL BLOCK DIAGRAM



Notes:

1. ZQ resistors are 240 Ohms +/-1% unless otherwise noted.
2. DQ to I/O wiring may be changed within a byte.
3. DQ, DQS, /DQS, ODT, DM, CKE and /S relationships must be maintained as shown.
4. /S2 and /S3 are not connected.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol; I^2C; Current sink capability of SDA driver ≤ 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
0	Number of SPD Bytes Written SPD Device Size CRC Coverage	Size = 256 CRC = 116 Bytes Used = 176	92h
1	SPD Revision	Revision 1.0	10h
2	Key Byte/DRAM Device Type	DDR3 SDRAM	0Bh
3	Key Byte/Module Type	UDIMM Width = 133.35mm Nom	02h
4	SDRAM Density and Banks	1Gb Density 8 Internal Banks	02h
5	SDRAM Device Row and Column Count	14 Rows 10 Columns	11h
6	Module Nominal Voltage, VDD	1.5V Operable Not 1.35V Operable	00h
7	Module Organization	2 Ranks x8 Device Width	09h
8	Module Memory Bus Width	8-Bit ECC 64-Bit Primary Bus Width	0Bh
9	Fine Timebase (FTB) Dividend/Divisor (Pico Seconds)	5/2 = 2.5ps	52h
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)	01h
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)	08h
12	SDRAM Minimum Cycle Time, $^tCK(min)$	1.5ns	0Ch
13	Reserved	-	00h
14	CAS Latencies Supported Least Significant Byte (LSB)	Low Byte CL Supported = 6, 7, 8, 9, 10	7Ch
15	CAS Latencies Supported Most Significant Byte (MSB)	High Byte CL Supported = 00h	00h
16	CAS Latency Time, $^tAA(min)$	13.5ns	6Ch
17	Write Recovery Time, $^tWR(min)$	15ns	78h
18	/RAS to /CAS Delay, $^tRCD(min)$	13.5ms	6Ch
19	Minimum Row Active to Row Active Delay Time, $^tRRD(min)$	6ns	30h
20	Minimum Row Precharge Time, $^tRP(min)$	13.5ns	6Ch
21	^tRAS and ^tRC Upper Nibbles	- -	11h
22	Min. Active to Precharge Delay Time, $^tRAS(min)$, LSB	36ns	20h
23	Min. Active to Active Refresh Delay Time, $^tRC(min)$, LSB	49.5ns	8Ch
24	Min. Refresh Recovery Delay Time, $^tRFC(min)$, LSB	110ns	70h
25	Min. Refresh Recovery Time, tRFC(min), MSB	110ns	03h
26	Min. Internal WRITE to READ Command Delay Time, $^tWTR(min)$	7.5ns	3Ch

Serial Presence Detect Information continued on next page.

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Serial PD Interface Protocol; I^2C; Current sink capability of SDA driver ≤ 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
27	Min. Internal READ to PRECHARGE Command Delay Time, $^tRTP(min)$	7.5ns	3Ch
28	Upper Nibble for ^tFAW	-	01h
29	Minimum Four Active Window Delay, $^tFAW(min)$, LSB	30ns	F0h
30	SDRAM Optional Features	DLL-Off Mode Support RZQ/7 Support	82h
31	SDRAM Thermal and Refresh Options	PASR/ODTS/ASR Unsupported Extended Temperature Range	01h
32	Module Thermal Sensor	00h = No Thermal Sensor	00h
33	SDRAM Device Type	00h = Standard Monolithic	00h
34 - 59	-	-	00h
60	Module Nominal Height	29 < Height ≤ 30mm	0Fh
61	Module Maximum Thickness	Back: 1 < Thickness ≤ 2mm Front: 1 < Thickness ≤ 2mm	11h
62	Reference Raw Card Used	Raw Card E, Rev. 00	04h
63	Address Mapping, 1st Rank, Edge Connector to DRAM	Mirrored	01h
64 - 116	Reserved	-	xxh
117 118	Module Manufacturer's JEDEC ID Code	STEC	01h A8h
119	Module ID: Module Manufacturing Location	01h = USA 02h = Malaysia	01h/02h
120 121	Module ID: Module Manufacturing Date		Varies per Build
122 123 124 125	Module ID: Module Serial Number		Unique per Module
126 127	Cyclical Redundancy Code		JEDEC Calculation

Serial Presence Detect Information continued on next page.

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Serial PD Interface Protocol; I^2C; Current sink capability of SDA driver ≤ 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
128	Module Part Number	7	37h
129		2	32h
130		Y	59h
131		8	38h
132		W	57h
133		2	32h
134		5	35h
135		6	36h
136		M	4Dh
137		8	38h
138		M	4Dh
139		-	2Dh
140		A	41h
141		1	31h
142		5	35h
143		L	4Ch
144		T	54h
145		G	47h
146	Module Revision Code		xxh
147			xxh
148	DRAM Manufacturer's JEDEC ID Code	JEP-106	Varies per DRAM Manufacturer
149			
150-175	Manufacturer's Specific Data		00h
176-255	Open for Customer Use		00h

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages and temperatures for extended periods may affect device reliability.

Symbol	Parameter		Minimum	Maximum	Units
V_{DD}	V_{DD} Supply Voltage relative to V_{SS}		-0.4	1.975	V
V_{DDQ}	V_{DDQ} Supply Voltage relative to V_{SS}		-0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any Pin relative to V_{SS}		-0.4	1.975	V
I_I	Input Leakage Current; Any input 0V <= V_{IN} <= V_{DD}; V_{REF} Input 0V <= V_{IN} <= 0.95V; (All other pins not under test = 0V)	Command/Address	-36	36	µA
		/S, CKE, ODT	-18	18	µA
		CK, /CK	-18	18	µA
		DM	-4	4	µA
I_{OZ}	Output Leakage Current; 0V <= V_{OUT} <= V_{DDQ}; DQS and ODT are disabled	DQ, DQS, /DQS	-10	10	µA
I_{VREF}	V_{REF} Leakage Current; V_{REF} = Valid V_{REF} Level		-18	-18	µA
I_{VTT}	Termination Reference Current from V_{TT}		-600	+600	mA
V_{TT}	Termination Reference Voltage-Command Address Bus ($\pm$ 20mV)		-0.49 x V_{DD}	+0.51 x V_{DD}	V
T_{STG}	Storage Temperature		-55	100	°C
T_C	Operating Temperature-DRAM Components				
	Commercial Operating Temperature		0	95	°C
	Industrial Operating Temperature: (W) Option		N/A	N/A	°C
T_A	Operating Temperature-Module, Ambient				
	Commercial Operating Temperature		0	70	°C
	Industrial Operating Temperature: (W) Option		N/A	N/A	°C

Notes:

1. Case Temperature, T_C, and Ambient Temperature, T_A, are simultaneous requirements.
2. Case Temperature, T_C, is the surface temperature on the center/top side of the DRAM. Please refer to the JESD51.2 Standard for the measurement conditions.
3. Case temperature range between 0°C to 85°C is the range which all DRAM specifications are supported.
4. For case temperature ranges between 85°C to 95°C, a doubling of the refresh commands in frequency to a 32ms period (^tREFI = 3.9µs) is required. To enter self-refresh mode at this temperature range, an EMRS command is required to change the internal refresh rate.

RECOMMENDED DC OPERATING CONDITIONS

All voltages referenced to V_{SS}.

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1
V_{DDQ}	I/O Supply Voltage	1.425	1.5	1.575	V	4
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51 x V_{DDQ}	V	2
V_{TT}	I/O Termination Voltage (System)	V_{REF} - 40	V_{REF}	V_{REF} + 40	mV	3

Notes:

1. V_{DD} and V_{DDQ} must track each other. V_{DDQ} must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-Peak noise (non-common mode) on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-Peak AC noise on VREF may not exceed ±2 percent of V_{REF}(DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{DDQ} tracks with V_{DD}; V_{DDL} tracks with V_{DD}.

INPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

INPUT DC LOGIC LEVELS

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IH}(DC)	Input High (Logic 1) Voltage	V_{REF} + 100	TBD	mV	1
V_{IL}(DC)	Input Low (Logic 0) Voltage	-TBD	V_{REF} - 100	mV	1
V_{REFDQ}(DC)	I/O Reference Voltage (DQ)	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	2, 3
V_{REFCA}(DC)	I/O Reference Voltage (CMD/ADD)	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	2, 3
V_{TT}	Termination Voltage	$V_{DDQ}/2$ - TBD	$V_{DDQ}/2$ + TBD	V	2, 3

INPUT AC LOGIC LEVELS

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IH}(AC)	Input High (Logic 1) Voltage	V_{REF} + 175	-	mV	1, 2
V_{IL}(AC)	Input Low (Logic 0) Voltage	-	V_{REF} - 175	mV	1, 2

DIFFERENTIAL INPUT LOGIC LEVELS

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IH}diff	Differential Input High Logic	+200	-	mV	
V_{IL}diff	Differential Input Low Logic	-	-200	mV	
V_{IX}	Differential Cross-Point Voltage relative to $V_{DD}/2$	-150	150	mV	

Notes:

1. For DQ and DM, V_{REF} = V_{REFDQ}. For input only pins except RESET, or V_{REF} = V_{REFCA}.
2. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than ±1% V_{DD} (approximately ±15mV for reference).
3. Approximately $V_{DD}/2$ ±15mV.

OUTPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

AC OUTPUT LEVELS

Symbol	Parameter	Value	Units	Notes
V_{OH}(AC)	AC Output High Measurement Level (SR Output)	V_{TT} + 0.1 x V_{DDQ}	V	1
V_{OL}(AC)	AC Output Low Measurement Level (SR Output)	V_{TT} - 0.1 x V_{DDQ}	V	1

DC OUTPUT LEVELS

Symbol	Parameter	Value	Units	Notes
V_{OH}(DC)	DC Output High Measurement Level (IV Curve Linearity)	0.8 x V_{DDQ}	V	
V_{OM}(DC)	DC Output Mid Measurement Level (IV Curve Linearity)	0.5 x V_{DDQ}	V	
V_{OL}(DC)	DC Output Low Measurement Level (IV Curve Linearity)	0.2 x V_{DDQ}	V	

DIFFERENTIAL AC and DC OUTPUT PARAMETERS

Symbol	Parameter	Value	Units	Notes
V_{OH}diff(AC)	AC Differential Output High Measurement Level (SR Output)	+0.2 x VDDQ	V	2
V_{OL}diff(DC)	AC Differential Output Low Measurement Level (SR Output)	-0.2 x VDDQ	V	2

Notes:

1. The swing of $\pm$0.1 x V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 ohms and an effective test load of 25 ohms to V_{TT} = V_{DDQ}/2.
2. The swing of +0.2 x V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 ohms and an effective test load of 25 ohms to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

IDD SPECIFICATIONS AND CONDITIONS

IDD specifications are tested after the device is properly initialized. Recommended Operating Temperature Range. V_{DD} = +1.5V ±0.075V, V_{DDQ} = +1.5V ±0.075V, V_{DDL} = +1.5V ±0.075V, V_{REF} = V_{DDQ}/2.

Input slew rate is specified by AC Parametric Test Conditions. IDD parameters are specified with ODT disabled. Data bus consists of DQ, DQS, and /DQS. IDD values must be met with all combinations of EMR bits 10 and 11.

IDDs IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET IDD6TC and IDD7 *are measured as time-averaged currents with all V_{DD} balls of the DDR3 SDRAM under test tied together*. Any IDDQ current is not included in IDD currents.

IDDs IDDQ2NT and IDDQ4R *are measured time-averaged currents with all V_{DDQ} balls of the DDR3 SDRAM under test tied together*. Any IDD current is not included in IDDQ currents.

Note: The user cannot use the IDDQ values to calculate DDR3 SDRAM power directly; the values can only be used to correlate simulated I/O power versus actual I/O power. IDDQ cannot be measured separately since V_{DD} and V_{DDQ} use a merged power layer in the PCB (module) design.

Definitions and parameters for IDD Conditions:

- LOW or 0 (zero) is defined as $V_{IN} \leq V_{IL}$AC) (MAX).
- HIGH or 1 (one) is defined as $V_{IN} \geq V_{IH}$(AC) (MIN).
- STABLE is defined as inputs stable at a HIGH or LOW level.
- FLOATING is defined as inputs at V_{REF} = V_{DDQ}/2.
- SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for *address and control signals*; also defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for *DQ signals* not including masks or strobes.
- R_{ON} = RZQ/7 (34 Ohms in MR1).
- R_{TT_NOM} = RZQ/6 (40 Ohms in MR1).
- R_{TT_WR} = RZQ/2 (120 Ohms in MR2).
- Q_{OFF} = Enabled in MR1.
- OTD = Enabled is enabled in MR1 and MR2.
- TDQS = Disabled in MR1.
- External DQ/DQS/DM load resister is 25 Ohms to V_{DDQ}/2.
- Burst Lengths are BL8 fixed.
- AL equals 0 (zero).
- ASR (optional) is disabled.

TIMING PARAMETERS - IDD MEASUREMENTS - CLOCKS

The following table lists the parameters used when measuring the IDD values.

IDD Parameter		DDR3-1333	Units
tCK(MIN)		1.5	ns
CL(IDD)		9	tCK
tRCD(MIN)		9	tCK
tRC(MIN)		33	tCK
tRAS(MIN)		24	tCK
tRP(MIN)		9	tCK
tFAW(IDD)	x4/x8	20	tCK
	x16	N/A	
tRRD(IDD)	x4/x8	4	tCK
	x16	N/A	
tRFC(IDD)	512Mb	N/A	tCK
	1Gb	74	
	2Gb	N/A	
	4Gb	N/A	

DDR3 IDD SPECIFICATIONS AND CONDITIONS

Symbol	Parameter/Condition
I_{DD0}	**Operating One Bank Active-Precharge Current**
	CKE = HIGH; External Clock = ON; $t_{CK(MIN)}$; $t_{RC(MIN)}$; $t_{RAS(MIN)}$; CL(IDD); BL = Note 1; /CS = HIGH between ACTIVATE and PRECHARGE; Command, Address, Bank Address Inputs = SWITCHING with exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Cycling with one bank active at a time; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
I_{DD1}	**Operating One Bank Active-Precharge Current**
	CKE = HIGH; External Clock = ON; $t_{CK(MIN)}$; $t_{RC(MIN)}$; $t_{RAS(MIN)}$; CL(IDD); BL = Note 1; /CS = HIGH between ACTIVATE, READ and PRECHARGE; Command Inputs = SWITCHING with exception of ACTIVATE and PRECHARGE commands; Row/Column Addresses = Row Addresses SWITCHING; Address A10 = LOW; Bank Address = Fixed; Data I/O = Read Data: Output Data switches after every clock cycle; Read Data is STABLE during falling DQS; I/O should be FLOATING when no data read; Output Buffer DQ, DQS = OFF; ODT = DISABLED; Active Banks = Bank 0; ACTIVATE to READ to PRECHARGE Loop.
I_{DD2N}	**Precharge Standby Current**
	CKE = HIGH; External Clock = ON; t_{CK} = $t_{CK(MIN)}$; /CS = STABLE at 1; All Device Banks = IDLE; Command Inputs = STABLE; Row/Column Addresses = STABLE; Bank Addresses = STABLE; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
I_{DD2NT}	**Precharge Standby ODT Current**
	CKE = HIGH; External Clock = ON; $t_{CK(MIN)}$, CL(IDD); BL = Note 1; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = DISABLED; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
I_{DDQ2NT}	**Precharge Standby ODT IDDQ Current (Optional)**
	See definition for I_{DD2NT}, but measuring IDDQ current rather than IDD current.
I_{DD2P_0}	**Precharge Power-Down Current - Slow Exit**
	CKE = HIGH; External Clock = ON; t_{CK} = $t_{CK(MIN)}$, CL(IDD); /CS = STABLE at 1; BL = Note 1; Command, Address, Bank Address Inputs = STABLE at 0; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Precharge Power Down Mode = Slow Exit, See Note 3.
I_{DD2P_1}	**Precharge Power-Down Current - Fast Exit**
	CKE = HIGH; External Clock = ON; t_{CK} = $t_{CK(MIN)}$, CL(IDD); /CS = STABLE at 1; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Precharge Power-Down Mode = Fast Exit, See Note 3.

DDR3 IDD Specifications and Conditions continued on next page.

DDR3 IDD SPECIFICATIONS AND CONDITIONS *(continued)*

Symbol	Parameter/Condition
I_{DD2Q}	**Precharge Quiet Standby Current**
	CKE = HIGH; External Clock = ON; ^tCK = $^tCK(MIN)$, CL(IDD); /CS = STABLE at 1; Command, Address, Bank Address Inputs = STABLE at 0; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0.
I_{DD3N}	**Active Standby Current**
	CKE = HIGH; External Clock = ON; ^tCK = $^tCK(MIN)$, CL(IDD); /CS = STABLE at 1; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Open; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
I_{DD3P}	**Active Power-Down Current**
	CKE = LOW; External Clock = ON; ^tCK = $^tCK(MIN)$, CL(IDD); BL = Note 1; /CS = STABLE at 1; Command, Address, Bank Address Inputs = STABLE at 0; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Open; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0.
I_{DD4R}	**Operating Burst Read Current**
	CKE = HIGH; External Clock = ON; ^tCK = $^tCK(MIN)$, CL(IDD); BL = Note 1; /CS = HIGH between READ; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = Read Data Burst (BL8): OUTPUT DATA switches after every clock cycle, read data is STABLE during falling DQS; DM = STABLE at 0; Bank Activity = All Banks open; READ Commands Cycling Through Banks; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
I_{DDQ4R}	**Operating Burst IDDQ Current (Optional)**
	See definition for I_{DD4R}, but measuring IDDQ current rather than IDD current.
I_{DD4W}	**Operating Burst Write Current**
	CKE = HIGH; External Clock = ON; ^tCK = $^tCK(MIN)$, CL(IDD); BL = Note 1; AL = 0; /CS = HIGH between WRITE; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = Write Data Burst (BL8): OUTPUT DATA switches after every clock cycle, read data is STABLE during falling DQS; DM = STABLE at 0; Bank Activity = All Banks Open; Write Commands Cycling Through Banks; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at HIGH; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
I_{DD5B}	**Burst Refresh Current**
	CKE = HIGH; External Clock = ON; ^tCK = $^tCK(MIN)$, ^tRC = $^tRC(MIN)$, CL(IDD), ^tRFC; BL = Note 1; AL = 0; /CS = HIGH between REFRESH; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = REFRESH command for every ^tRFC; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.

DDR3 IDD Specifications and Conditions continued on next page.

DDR3 IDD SPECIFICATIONS AND CONDITIONS *(continued)*

Symbol	Parameter/Condition
I_{DD6}	**Self-Refresh Current - Normal Temperature Range: T_C = 0°C - 85°C**
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED, See Note 4; Self-Refresh Temperature Range (SRT) = NORMAL, See Note 5; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD6ET}	**Self-Refresh Current - Extended Temperature Range: T_C = 0°C - 95°C (Optional)**
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED; Self-Refresh Temperature Range (SRT) = EXTENDED, See Note 4; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Extended Temperature Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD6TC}	**Auto Self-Refresh Current - T_C = 0°C - 95°C (Optional)**
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED, See Note 4; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Auto Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD7}	**Operating Bank Interleave Read Current**
	CKE = HIGH; External Clock = ON; ^tCK = $^tCK(MIN)$; ^tRC = $^tRC(MIN)$; ^tRAS = $^tRAS(MIN)$; ^tRCD = $^tRCD(MIN)$; CL(IDD); BL = Note 1; AL = 0; /CS = HIGH between Valid Commands; Row/Column Addresses = STABLE between DESELECTs (DES); Data I/O = Read Data (BL8): Output Data Switches after every Clock Cycle; Read Data is STABLE while DQS is falling; DM = STABLE at 0; Bank Activity = Interleaving Reads Cycling Through Banks; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.

Notes:
1. BL (Burst Length) = BL8, fixed by MRS; set to MR0 A[1,0] = 00B.
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_WR enable: set MR2 A[10,9] = 10B.
3. Precharge Power Down Mode: set MR0 A12 = 0B for Slow Exit or MR0 A12 = 1B for Fast Exit.
4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature.
5. Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for Normal or 1B for Extended Temperature Range.
6. Refer to SDRAM supplier/manufacturer datasheet and/or DIMM SPD to determine if optional features or requirements are supported by the DDR3 SDRAM device.

DDR3 IDD SPECIFICATIONS AND CONDITIONS *(continued)*

Symbol	Parameter/Condition
I_{DD6}	**Self-Refresh Current - Normal Temperature Range: T_C = 0°C - 85°C**
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED, See Note 4; Self-Refresh Temperature Range (SRT) = NORMAL, See Note 5; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD6ET}	**Self-Refresh Current - Extended Temperature Range: T_C = 0°C - 95°C (Optional)**
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED; Self-Refresh Temperature Range (SRT) = EXTENDED, See Note 4; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Extended Temperature Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD6TC}	**Auto Self-Refresh Current - T_C = 0°C - 95°C (Optional)**
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED, See Note 4; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Auto Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD7}	**Operating Bank Interleave Read Current**
	CKE = HIGH; External Clock = ON; t_{CK} = $t_{CK(MIN)}$; t_{RC} = $t_{RC(MIN)}$; t_{RAS} = $t_{RAS(MIN)}$; t_{RCD} = $t_{RCD(MIN)}$; CL(IDD); BL = Note 1; AL = 0; /CS = HIGH between Valid Commands; Row/Column Addresses = STABLE between DESELECTs (DES); Data I/O = Read Data (BL8): Output Data Switches after every Clock Cycle; Read Data is STABLE while DQS is falling; DM = STABLE at 0; Bank Activity = Interleaving Reads Cycling Through Banks; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.

Notes:

1. BL (Burst Length) = BL8, fixed by MRS; set to MR0 A[1,0] = 00B.
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_WR enable: set MR2 A[10,9] = 10B.
3. Precharge Power Down Mode: set MR0 A12 = 0B for Slow Exit or MR0 A12 = 1B for Fast Exit.
4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature.
5. Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for Normal or 1B for Extended Temperature Range.
6. Refer to SDRAM supplier/manufacturer datasheet and/or DIMM SPD to determine if optional features or requirements are supported by the DDR3 SDRAM device.

MAXIMUM DDR3 IDD VALUES

Notes:

1. For a one rank module:

   IDD*n* is calculated with the rank in IDD*n*.

   For two rank modules:

   1. IDD0, IDD1, IDD4W, IDD4R, IDD5 and IDD7 are calculated with one rank in IDD*n* and one rank in IDD2N **and**
   2. IDD2P, IDD2Q, IDD2N, IDD3P, IDD3N and IDD6 are calculated with two ranks in IDD*n*.

   For four rank modules:

   1. IDD0, IDD1, IDD4W, IDD4R, IDD5 and IDD7 are calculated with one rank in IDD*n* and one rank in IDD2N and two ranks in IDD2P, **and**
   2. IDD2P, IDD2Q, IDD2N, IDD3P, IDD3N and IDD6 are calculated with two ranks in IDD*n* and two ranks in IDD2P.

   Where *n* = corresponding IDD condition listed in the Symbol column.
3. Values shown for DDR3 SDRAM components only.
4. Values will differ according to the DRAM parts used to manufacture the module.
5. IDD values are calculated using worst-case specifications of currently available DRAMs from different manufacturers.
6. For Industrial Operating Temperature Range:

   When $T_C \leq 0^oC$:

   1. IDD2P and IDD3P must be derated by 4 percent
   2. IDD4R and IDD5W must be derated by 2 percent
   3. IDD6 and IDD7 must be derated by 7 percent

   When $T_C \leq 85^oC$:

   1. IDD0, IDD1, IDD2N, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W and IDD5B must be derated by 2 percent
   2. IDD2P must be derated by 20 percent
   3. IDD3P must be derated by 30 percent
   4. IDD6 must be derated by 80 percent (IDD6 will increase by this amount if $T_C < 85^oC$ and the 2x refresh option is still enabled)

Symbol	DDR3-1333	Units
I_{DD0}	1,510	mA
I_{DD1}	1,690	mA
I_{DD2N}	1,170	mA
I_{DD2NT}	1,530	mA
I_{DDQ2NT}	(Optional)	mA
I_{DD2P_0}	216	mA
I_{DD2P_1}	720	mA
I_{DD2Q}	1,080	mA
I_{DD3N}	1,116	mA
I_{DD3P}	720	mA
I_{DD4R}	2,320	mA
I_{DDQ4R}	(Optional)	mA
I_{DD4W}	2,500	mA
I_{DD5B}	2,680	mA
I_{DD6}	180	mA
$I_{DD6_{ET}}$	(Optional)	mA
$I_{DD6_{TC}}$	(Optional)	mA
I_{DD7}	4,930	mA

SPEED BINS - DDR3-1333

Recommended Operating Temperature Range; $V_{DDQ} = V_{DD} = 1.5V \pm 0.075V$

Symbol	Parameter		Minimum	Maximum	Units
^{t}RCD	ACT to Internal READ or WRITE Delay Time		13.50	-	ns
^{t}RP	PRECHARGE Command Period		13.50	-	ns
^{t}RC	ACT to ACT or REF Command Period		49.50	-	ns
^{t}RAS	ACT to PRE Command Period		36.00	9 x ^{t}REFI	ns
^{t}CK(avg)	CL = 5	CWL = 5	Reserved		ns
		CWL = 6, 7	Reserved		ns
	CL = 6	CWL = 5	2.5	3.3	ns
		CWL = 6	Reserved		ns
		CWL = 7	Reserved		ns
	CL = 7	CWL = 5	Reserved		ns
		CWL = 6	1.875	< 2.5	ns
		CWL = 7	Reserved		ns
	CL = 8	CWL = 5	Reserved		ns
		CWL = 6	1.875	< 2.5	ns
		CWL = 7	Reserved		ns
	CL = 9	CWL = 5, 6	Reserved		ns
		CWL = 7	1.5	< 1.875	ns
	CL = 10	CWL = 5, 6	Reserved		ns
		CWL = 7	1.5	< 1.875	ns
	Supported CL Settings		6, 7, 8, 9, 10		CK
	Supported CWL Settings		5, 6, 7		CK

SPEED BIN NOTES

1. The CL and CWL settings result in ^{t}CK(AVG).MIN and ^{t}CK(AVG).MAX requirements. When selecting a ^{t}CK(AVG), both need to be fulfilled.
2. ^{t}CK(AVG).MIN limits. CAS Latency is not strictly analog; the data and strobe output are synchronized by the DLL. All possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard ^{t}CK(AVG) value (2.5, 1.875, 1.5 or 1.25 nanoseconds) when calculating CL [*n*CK] = ^{t}AA[ns], rounding up to the next 'supported CL'.
3. ^{t}CK(AVG).MAX limits: ^{t}CK(AVG) = ^{t}AA.MAX/ CLSELECTED, rounding the ^{t}CK(AVG) down to the next valid speed bin limit (3.3ns or 2.5ns, or 1.875ns or 1.25ns). This result is ^{t}CK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. The user must program a different value.
5. 'Optional' settings allow certain devices to support this setting, but it is not a mandatory feature. Refer to the datasheet of the supplier and SPD information to determine if and how this setting is supported.
6. Any DDR3 speed bin also supports functional operation at lower frequencies as indicated in the table but are verified by design only and not production tests.
7. ^{t}REFI is dependent on T_C operating temperature (case temperature).

Speed Bins continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS

Clock Timing

Symbol	Parameters		Minimum	Maximum	Units
tCKDLL_DIS	Clock Period Average: DLL Disable Mode	T_C = 0°C to 85°C	8	7,800	ns
		T_C = >85°C to 95°C	8	3,900	ns
tCK (AVG)	Clock Period Average: DLL Enable Mode	See the SPEED BINS Table for the tCK Range.			ns
tCH (AVG)	High Pulse Width Average	-	0.47	0.53	CK
tCL (AVG)	Low Pulse Width Average	-	0.47	0.53	CK
tJITPER	Clock Period Jitter	DLL Locked	-80	80	ps
tJITPER, LCK	Clock Period Jitter	DLL Locking	-70	70	ps
tCK (ABS)	Clock Absolute Period	-	tCK(AVG) MIN + tJITPER MIN	tCK(AVG) MAX + tJITPER MAX	ps
		-			

Clock Jitter

Symbol	Parameters		Minimum	Maximum	Units
tJITCC	Cycle-to-Cycle Jitter	DLL Locked	160		ps
tJITCC, LCK	Cycle-to-Cycle Jitter	DLL Locking	140		
tERR2PER	Cumulative Error	2 Cycles	-118	118	ps
tERR3PER	Cumulative Error	3 Cycles	-140	140	ps
tERR4PER	Cumulative Error	4 Cycles	-155	155	ps
tERR5PER	Cumulative Error	5 Cycles	-168	168	ps
tERR6PER	Cumulative Error	6 Cycles	-177	177	ps
tERR7PER	Cumulative Error	7 Cycles	-186	186	ps
tERR8PER	Cumulative Error	8 Cycles	-193	193	ps
tERR9PER	Cumulative Error	9 Cycles	-200	200	ps
tERR10PER	Cumulative Error	10 Cycles	-205	205	ps
tERR11PER	Cumulative Error	11 Cycles	-210	210	ps
tERR12PER	Cumulative Error	12 Cycles	-215	215	ps
tERR*n*PER	*n* = 13, 14...49, 50	*n* Cycles	tERR*n*PER MIN = (1 + 0.68ln[*n*]) x tJITPER MIN	tERR*n*PER MAX = (1 + 0.68ln[*n*]) x tJITPER MAX	ps

DQ Input Timing

Symbol	Parameters		Minimum	Maximum	Units
tDSAC175	Data Setup Time to DQS, /DQS	Base (Specification)	-	-	ps
		VREF @ 1 V/ns	-	-	
tDHAC175	Data Hold Time from DQS, /DQS	Base (Specification)	-	-	ps
		VREF @ 1 V/ns	-	-	
tDSAC150	Data Setup Time to DQS, /DQS	Base (Specification)	30	-	ps
		VREF @ 1 V/ns	180	-	
tDHAC150	Data Hold Time from DQS, /DQS	Base (Specification)	65	-	ps
		VREF @ 1 V/ns	165	-	
tDIPW	Minimum Data Pulse Width	-	400	-	ps

AC Operating Conditions and Electrical Parameters continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS *(Continued)*

DQ Output Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
^{t}DQSQ	DQS, /DQS to DQ Skew	Per Access	-	125	ps
^{t}QH	DQ Output Hold Time from DQS, /DQS	-	0.38	-	ps
^{t}LZ (DQ)	DQ Low-Z Time from CK, /CK	-	-500	250	ps
^{t}HZ (DQ)	DQ High-Z Time from CK, /CK	-	-	250	ps
DQ Strobe Input Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
^{t}DQSS	DQS, /DQS Rising to CK, /CK Rising		-0.25	0.25	CK
^{t}DQSL	DQS, /DQS Differential Input Low Pulse Width		0.45	0.55	CK
^{t}DQSH	DQS, /DQS Differential Input High Pulse Width		0.45	0.55	CK
^{t}DSS	DQS, /DQS Falling Setup to CK, /CK Rising		0.2	-	CK
^{t}DSH	DQS, /DQS Falling Hold from CK, /CK Rising		0.2	-	CK
^{t}WPRE	DQS, /DQS Differential WRITE Preamble		0.9	-	CK
^{t}WPST	DQS, /DQS Differential WRITE Postamble		0.3	-	CK
DQ Strobe Output Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
^{t}DQSCK	DQS, /DQS Rising To/From Rising CK, /CK		-255	255	ps
^{t}DQSCKDLL_DIS	DQS, /DQS Rising To/From Rising CK, /CK when DLL is disabled.		1	10	ns
^{t}QSH	DQS, /DQS Differential Output High Time		0.40	-	CK
^{t}QSL	DQS, /DQS Differential Output Low Time		0.40	-	CK
^{t}LZ (DQS)	DQS, /DQS Low-Z Time (RL - 1)		-500	250	ps
^{t}HZ (DQS)	DQS, /DQS High-Z Time (RL + BL/2)		-	250	ps
^{t}RPRE	DQS, /DQS Differential READ Preamble		0.9	-	CK
tRPST	DQS, /DQS Differential READ Postamble		0.3	-	CK
Command and Address Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
^{t}DLLK	DLL Locking Time	-	512	-	CK
^{t}ISAC175	CTRL, CMD, ADDR Setup to CK, /CK	Base (Specification)	65	-	ps
		VREF @ 1 V/ns	240	-	ps
^{t}IH	CTRL, CMD, ADDR Hold from CK, /CK	Base (Specification)	140	-	ps
		VREF @ 1 V/ns	240	-	ps
^{t}ISAC150	CTRL, CMD, ADDR Setup to CK, /CK	Base (Specification)	190	-	ps
		VREF @ 1 V/ns	340	-	ps
^{t}IPW	CTRL, CMD, ADDR Minimum Pulse Width		780	-	ps
^{t}RCD	ACTIVATE to Internal READ or WRITE Delay		See the Speed Bins Table for ^{t}RCD.		ns
^{t}RP	PRECHARGE Command Period		See the Speed Bins Table for ^{t}RP.		ns
^{t}RAS	ACTIVATE-to-PRECHARGE Command Period		See the Speed Bins Table for ^{t}RAS.		ns
^{t}RC	ACTIVATE-to-ACTIVATE Command Period		See the Speed Bins Table for ^{t}RC.		ns
^{t}RRD	ACTIVATE-to-ACTIVATE Minimum Command Period	1KB Page Size	MIN = > of 4CK or 6ns		CK
		2KB Page Size	MIN = > of 4CK or 10ns (N/A)		CK

AC Operating Conditions and Electrical Parameters continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS *(Continued)*

Symbol	Parameters		Minimum	Maximum	Units
Command and Address Timing *(continued)*					
^tFAW	Four ACTIVATE Windows	1 KB Page Size	30	-	ns
		2 KB Page Size	45 (N/A)	-	ns
^tWR	Write Recovery Time	-	15ns	N/A	ns
^tWTR	Delay from Start of Internal WRITE Transaction to Internal READ Command		> of 4CK or 7.5ns	N/A	CK
^tRTP	READ-to-PRECHARGE Time		> of 4CK or 7.5ns	N/A	CK
^tCCD	/CAS-to/CAS Command Delay		4CK	N/A	CK
^tDAL	Auto Precharge Write Recovery + Precharge Time		WR + ^tRP /^tCK (AVG)	N/A	CK
^tMRD	MODE REGISTER SET Command Cycle Time		4CK	N/A	CK
^tMOD	MODE REGISTER SET Command Update Delay		> of 12CK or 15ns	N/A	CK
^tMPRR	MULTIPURPOSE REGISTER READ Burst End to Mode Register Set for Multipurpose Register Exit		1CK	N/A	CK
Calibration Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
^tZQINIT	ZQCL Command: Long Calibration Time	POWER-UP and RESET	512	-	CK
^tZQOPER	ZQCL Command: Short Calibration Time	Normal Operation	256	-	CK
^tZQCS	ZQCS Command: Short Calibration Time		64	-	CK
Initialization and Reset Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
^tXPR	Exit Reset from CKE HIGH to a Valid Command		> of 5CK or ^tRFC + 10ns	N/A	CK
^tVDDPR	Power Supply Ramp to Power Supplies Stable		N/A	200	ms
^tRPS	/RESET LOW to Power Supplies Stable		0	200	ms
^tIOz	/RESET LOW to I/O and RTT High-Z		N/A	20	ns
Refresh Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
^tRFC	REFRESH-to-ACTIVATE or REFRESH Command Period		110	9 x ^tREFI	ns
	Maximum Refresh Period	T_C = 0°C to 85°C	64 (1X)		ms
		T_C = > 85°C to 95°C	32 (2X)		ms
^tREFI	Maximum Average Periodic Refresh	T_C = 0°C to 85°C	7.8 (64ms/8,192)		µs
		T_C = > 85°C to 95°C	3.9 (32ms/8,192)		µs

AC Operating Conditions and Electrical Parameters continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS *(Continued)*

Self-Refresh Timing

Symbol	Parameters	Minimum	Maximum	Units
^{t}XS	Exit Self-Refresh to commands not requiring a locked DLL	> of 5CK or ^{t}RFC + 10ns	N/A	CK
^{t}XSDLL	Exit Self-Refresh to commands that require a locked DLL	^{t}DLLK (MIN)	N/A	CK
^{t}CKESR	Minimum CKE Low Pulse Width for Self-Refresh Entry to Self-Refresh Exit Timing	^{t}CKE (MIN) + CK	N/A	CK
^{t}CKSRE	Valid Clocks after Self-Refresh Entry or Power-Down Entry	> of 5CK or 10ns	N/A	CK
^{t}CKSRX	Valid Clocks b/f Self-Refresh Exit, Power-Down Exit, or Reset Exit	> of 5CK or 10ns	N/A	CK

Power-Down Timing

Symbol	Parameters	Minimum	Maximum	Units
^{t}CKE	CKE MIN Pulse Width	> of 3CK or 5.625ns		CK
^{t}CPDED	Command Pass Disable Delay	1	N/A	CK
^{t}PD	Power-Down Entry to Power-Down Exit Timing	^{t}CKE (MIN)	9 x ^{t}REFI	CK
^{t}ANPD	Begin Power-Down Period prior to CKE Registered HIGH	WL - 1CK		CK
PDE	Power-Down Entry Period; ODT synchronous/asynchronous	> of tANPD or ^{t}RFC - REFRESH Command to CKE LOW Time		CK
PDX	Power-Down Exit Period; ODT synchronous/asynchronous	^{t}ANPD + ^{t}XPDLL		CK

Power-Down Entry Minimum Timing

Symbol	Parameters		Minimum	Maximum	Units
^{t}ACTPDEN	ACTIVATE Command to Power-Down Entry		1	-	CK
tPRPDEN	PRECHARGE/PRECHARGE ALL Command to Power-Down Entry		1	-	CK
^{t}REFPDEN	REFRESH Command to Power-Down Entry		1	-	CK
^{t}MRSPDEN	MRS Command to Power-Down Entry		^{t}MOD (MIN)	-	CK
^{t}RDPDEN	READ/READ with Auto-Precharge Command to Power-Down Entry		RL + 4 + 1	-	CK
^{t}WRPDEN	WRITE Command to Power-Down Entry	BL8 (OTF, MRS) BC4OTF	WL + 4 + ^{t}WR/^{t}CK (AVG)	-	CK
		BC4MRS	WL + 2 + ^{t}WR/^{t}CK (AVG)	-	
^{t}WRAPDEN	WRITE with Auto-Precharge Command to Power-Down Entry	BL8 (OTF, MRS) BC4OTF	WL + 4 + WR + 1	-	CK
		BC4MRS	WL + 2 + WR + 1		

Power-Down Exit Timing

Symbol	Parameters		Minimum	Maximum	Units
^{t}XP	DLL ON, any valid command, or DLL OFF to commands not requiring a locked DLL		> of 3CK or 6ns	N/A	CK
^{t}XPDLL	Precharge Power-Down with DLL OFF to commands that require a locked DLL		> of 10CK or 24ns	N/A	CK

AC Operating Conditions and Electrical Parameters continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS *(Continued)*

ODT Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
ODTL ON	RTT Synchronous Turn-On Delay		CWL + AL - 2CK		CK
ODTL OFF	RTT Synchronous Turn-Off Delay		CWL + AL - 2CK		CK
^{t}AON	RTT Turn-On from ODTL On Reference		-250	250	ps
^{t}AOF	RTT Turn-Off from ODTL Off Reference		0.3	0.7	CK
^{t}AONPD	Asynchronous RTT Turn-On Delay (Power-Down with DLL OFF)		1	9	ns
^{t}AOFPD	Asynchronous RTT Turn-Off Delay (Power-Down with DLL OFF)		1	9	ns
ODTH8	ODT HIGH Time with WRITE Command and BL8		6	N/A	CK
ODTH4	ODT HIGH Time without WRITE Command or with WRITE Command with BC4		4	N/A	CK
Dynamic ODT Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
ODTLCNW	RTT_NOM-to-RTT_WR Change Skew		WL - 2CK		CK
ODTLCNW4	RTT_NOM-to-RTT_WR Change Skew	BC4	4CK + ODTL Off		CK
ODTLCNW8	RTT_NOM-to-RTT_WR Change Skew	BL8	6CK + ODTL Off		CK
^{t}ADC	RTT Dynamic Change Skew		0.3	0.7	CK
Write-Leveling Timing					
Symbol	**Parameters**		**Minimum**	**Maximum**	**Units**
^{t}WLMRD	First DQS, /DQS Rising Edge		40	-	CK
^{t}WLDQSEN	DQS, /DQS Delay		25	-	CK
^{t}WLS	Write-Leveling Setup from rising CK, /CK crossing to rising DQS, /DQS crossing		245	-	ps
^{t}WLH	Write-Leveling Hold from rising DQS, /DQS crossing to rising CK, /CK crossing		245	-	ps
^{t}WLO	Write-Leveling Output Delay		0	9	ns
^{t}WLOE	Write-Leveling Output Error		0	2	ns

Notes:

1. It is recommended that the system designer or system engineer reference the latest specification release notes from the DRAM manufacturers in regards to these signals. The default operational characteristics are listed here for reference only.

REVISION HISTORY

Revision	Date	Description
-101	06/21/2007	Initial release.
-102	09/12/2007	Updated functional block diagram, SPD and general layout to latest specification.
-103	02/26/2009	Updated to Halogen-Free.
-104	08/21/2009	Updated to latest format.
-105	10/19/2009	SPD Bytes 128-145 corrected to BOM values.

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