

256M x 64 Bit (2GB) 204-Pin DDR3 SO-DIMM (PC3-10600) 2 Ranks x 8; RoHS-6 Compliant and Halogen-Free

GENERAL DESCRIPTION

The SL64F8W256M8L-A15LTG is a 256M x 64 bit (2GB) 204-pin Double Data Rate 3 (DDR3) Unbuffered Small Outline Dual In-Line Memory Module (SO-DIMM).

The module consists of sixteen CMOS 16M x 8 bit x 8 bank DDR3 SDRAMs in lead-free BGA packages mounted in 2 ranks on a 204-pin glass epoxy substrate.

A Serial Presence Detect and Thermal Sensor (SPD/TS) is mounted to provide the SPDs (using two pin I2C) and temperature digital word (JC42.4 compliant). Decoupling capacitors are mounted across the power supply. Damping resistors are added in series for DQ, DQS and DM signals.

The module has gold edge connections and is intended for mounting into 204-pin SO-DIMM edge connector sockets keyed for 1.5V.

FEATURES

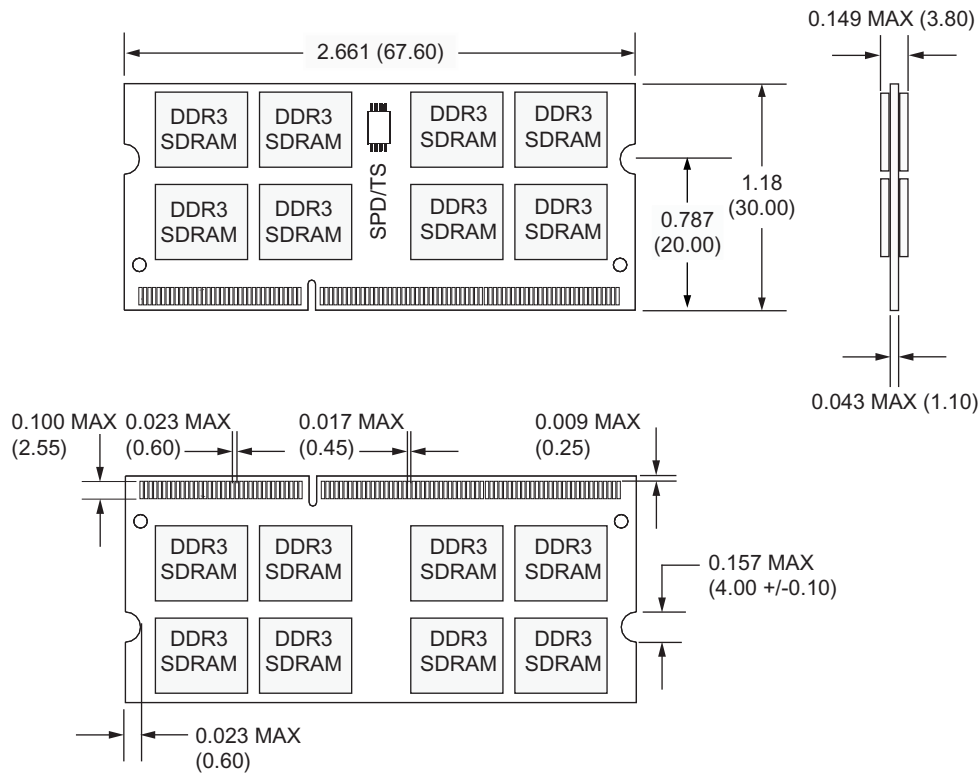
- PC3-10600 Compliant (DDR3-1333 667MHz-1.5ns@CL-^tRCD-^tRP: 9-9-9)
- 204-Pin SO-DIMM form factor
- Average Periodic Refresh Interval (^tREFI)
 - 7.8125ms Max for 0°C < T_C < 85°C (64ms/8,196 cycles)
 - 3.9ms Max for 85°C < T_C < 95°C (32ms/8,196 cycles)
- V_{DD} = V_{DDQ} = 1.5V ±0.075V
- V_{DDSPD} = 3.3V ±0.3V
- JEDEC Standard 1.5V I/O (SSTL_15 compatible)
- DDR3 Architecture: Two data accesses per clock cycle, differential clock inputs (CK, /CK), bidirectional differential data strobe (DQS, /DQS), Off-Chip Driver (OCD), Impedance Adjustment, Dynamic On-Die Termination (ODT), On-Chip Delay Locked Loop (DLL); Eight-bit prefetch architecture
- Commands entered on each rising CK edge; DQS-edge aligned with data for READs and center-aligned with data for WRITEs; DLL to align DQ and DQS transitions with CK
- Eight internal component banks for concurrent operation
- Asynchronous RESET Pin Support
- ZQ Calibration Support
- Concurrent Auto Precharge option is supported
- Data Mask (DM) for masking Write data
- Programmable Burst Lengths: 4 (Burst Chop) and 8 (Nibble Sequential and Interleave Mode)
- /CAS READ Latency (CL): 6, 8, 9, 10
- /CAS WRITE Latency (CWL): 5, 6, 7-^tCK
- Posted /CAS Additive Latency (AL): 0, CL-1, CL-2
- Adjustable Data-Output drive strength
- Serial Presence Detect/Thermal Sensor (SPD/TS)
- Gold edge contacts
- RoHS-6 Compliant and Halogen Free

ORDERING INFORMATION

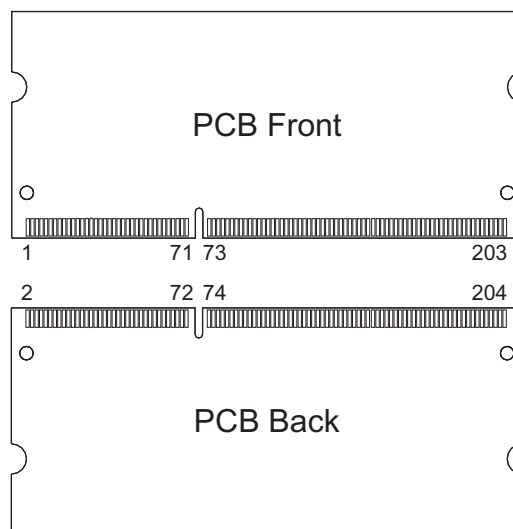
Part Number	Module Speed	DRAM Speed	CL- ^t RCD- ^t RP
SL64F8W256M8L-A15LTG	PC3-10600	DDR3-1333	9-9-9

PACKAGE DIMENSIONS (Board No. 1794)

Units are in inches (millimeters). All dimensions are typical unless otherwise noted.



PIN LOCATIONS



PIN CONFIGURATION (* = Not Used; / = Active Low; **Bold Line or Box** = Key)**204-PIN SO-DIMM PINOUT**

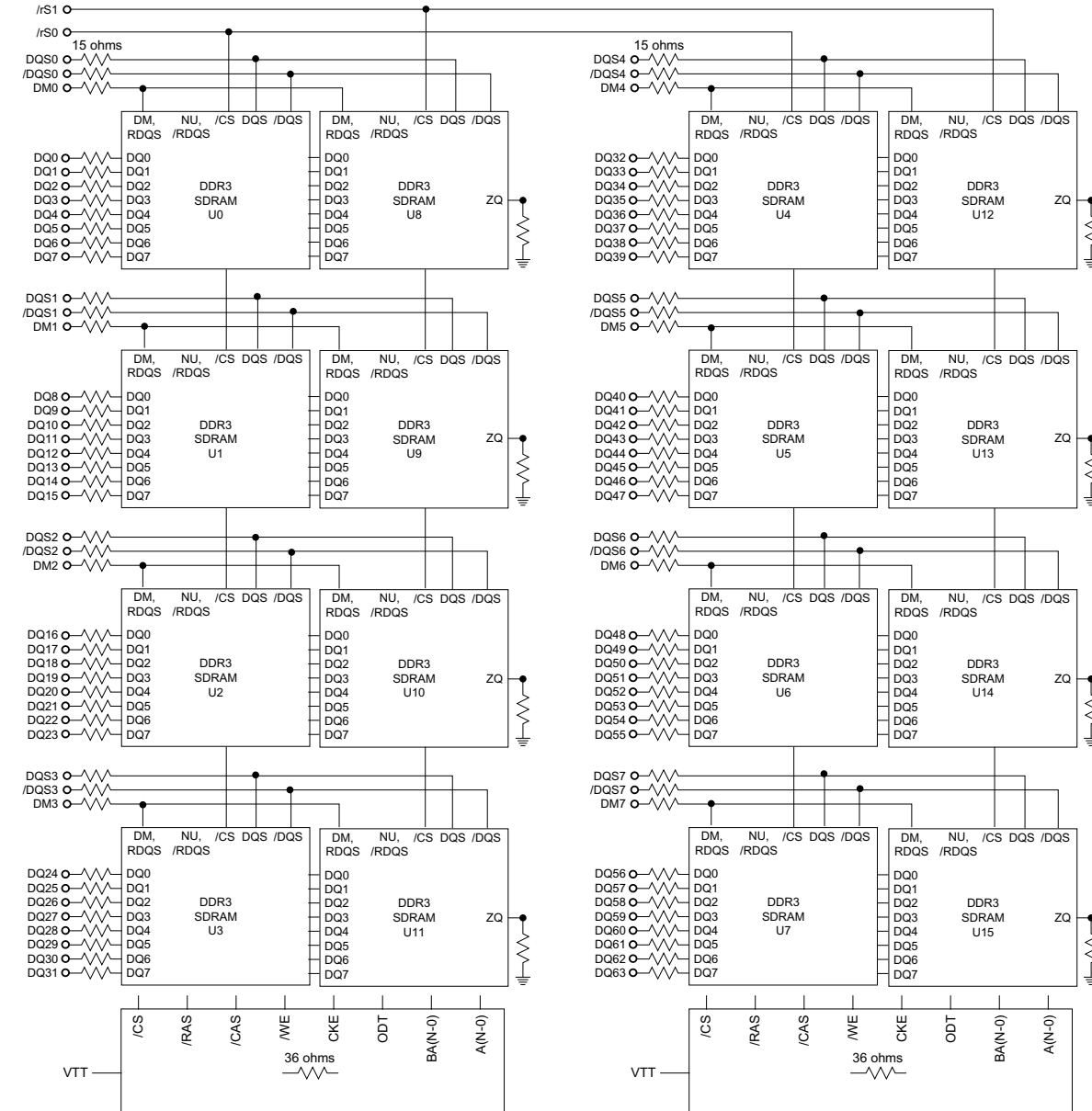
204-Pin SO-DIMM Front								204-Pin SO-DIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	53	DQ19	105	VDD	157	DQ42	2	VSS	54	VSS	106	VDD	158	DQ46
3	VSS	55	VSS	107	A10/AP	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	VSS	6	DQ5	58	DQ29	110	/RAS	162	VSS
7	DQ1	59	DQ25	111	VDD	163	DQ48	8	VSS	60	VSS	112	VDD	164	DQ52
9	VSS	61	VSS	113	/WE	165	DQ49	10	/DQS0	62	/DQS3	114	/S0	166	DQ53
11	DM0	63	DM3	115	/CAS	167	VSS	12	DQS0	64	DQS3	116	ODT0	168	VSS
13	VSS	65	VSS	117	VDD	169	/DQS6	14	VSS	66	VSS	118	VDD	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	ODT1	172	VSS
17	DQ3	69	DQ27	121	/S1	173	VSS	18	DQ7	70	DQ31	122	NC	174	DQ54
19	VSS	71	VSS	123	VDD	175	DQ50	20	VSS	72	VSS	124	VDD	176	DQ55
21	DQ8	73	CKE0	125	TEST	177	DQ51	22	DQ12	74	CKE1	126	VREFCA	178	VSS
23	DQ9	75	VDD	127	VSS	179	VSS	24	DQ13	76	VDD	128	VSS	180	DQ60
25	VSS	77	NC	129	DQ32	181	DQ56	26	VSS	78	A15*	130	DQ36	182	DQ61
27	/DQS1	79	BA2	131	DQ33	183	DQ57	28	DM1	80	A14*	132	DQ37	184	VSS
29	DQS1	81	VDD	133	VSS	185	VSS	30	/RESET	82	VDD	134	VSS	186	/DQS7
31	VSS	83	A12/VBC	135	/DQS4	187	DM7	32	VSS	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	VSS	34	DQ14	86	A7	138	VSS	190	VSS
35	DQ11	87	VDD	139	VSS	191	DQ58	36	DQ15	88	VDD	140	DQ38	192	DQ62
37	VSS	89	A8	141	DQ34	193	DQ59	38	VSS	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	VSS	40	DQ20	92	A4	144	VSS	196	VSS
41	DQ17	93	VDD	145	VSS	197	SA0	42	DQ21	94	VDD	146	DQ44	198	/EVENT
43	VSS	95	A3	147	DQ40	199	VDDSPD	44	VSS	96	A2	148	DQ45	200	SDA
45	/DQS2	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	VSS	202	SCL
47	DQS2	99	VDD	151	VSS	203	VTT	48	VSS	100	VDD	152	/DQS5	204	VTT
49	VSS	101	CK0	153	DM5			50	DQ22	102	CK1	154	DQS5		
51	DQ18	103	/CK0	155	VSS			52	DQ23	104	/CK1	156	VSS		

PIN CONFIGURATION (Continued) (* = Not Used; / = Active Low)**PIN FUNCTIONS**

Symbol	Type	Description
CK0, CK1	Input	Clock Inputs, Positive Line
/CK0, /CK1	Input	Clock Inputs, Negative Line
CKE0, CKE1	Input	Clock Enable
/RAS	Input	Row Address Strobe
/CAS	Input	Column Address Strobe
/WE	Input	Write Enable
/S0, /S1	Input	Chip Select
ODT0, ODT1	Input	On Die Termination
DM0-DM7	Input	Data Masks
DQS0-DQS7	Input/Output	Data Strobes
/DQS0-/DQS7	Input/Output	Data Strobes, Negative
DQ0-DQ63	Input/Output	Data Input/Output
BA0-BA2	Input	Bank Address Inputs
A0-A9, A11, A13, A14*, A15*	Input	Address Inputs
A10 /AP	Input	Address Input/Autoprecharge
A12 /BC	Input	Address Input/Burst Chop
CB0-CB7*	Input/Output	Data Check Bits
SCL	Input	Serial Clock for Presence Detect
SA0-SA1	Input	Presence Detect Address Inputs
SDA	Input/Output	Serial Presence Detect Data
/RESET	Input	Register and SDRAM Control
NC		No Connect (Reserved for Future Use)
/EVENT	Output	Overtemperature Event
TEST*		Memory Bus Test Tool (NC and not used for SO-DIMMs)
VDDSPD	Supply	Serial EEPROM/Temp. Sensor Power Supply: 3.3V \pm 0.3V
VDD	Supply	Core and I/O Power: 1.5V \pm 0.075V
VSS	Supply	Ground
VREFDQ	Supply	DQ Reference Voltage
VREFCA	Supply	CA Reference Voltage
VTT	Supply	Termination Voltage

FUNCTIONAL BLOCK DIAGRAM

DDR3 SDRAM DEVICES - 2 RANKS x 8



SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol; I²C; Current sink capability of SDA driver ≤ 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
0	Number of SPD Bytes Written SPD Device Size CRC Coverage	Size = 256 CRC = 116 Bytes Used = 176	92h
1	SPD Revision	Revision 1.0	10h
2	Key Byte/DRAM Device Type	DDR3 SDRAM	0Bh
3	Key Byte/Module Type	SO-DIMM Width = 67.6mm Nom	03h
4	SDRAM Density and Banks	1Gb Density 8 Internal Banks	02h
5	SDRAM Device Row and Column Count	14 Rows 10 Columns	11h
6	Module Nominal Voltage, VDD	1.5V / Not 1.35V Operable	00h
7	Module Organization	2 Ranks x8 Device Width	09h
8	Module Memory Bus Width	Non-ECC 64-Bit Primary Bus Width	03h
9	Fine Timebase (FTB) Dividend/Divisor (Pico Seconds)	5/2 = 2.5ps	52h
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)	01h
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)	08h
12	SDRAM Minimum Cycle Time, t _{CK} (min)	1.5ns	0Ch
13	Reserved	-	00h
14	CAS Latencies Supported Least Significant Byte (LSB)	Low Byte CL Supported = 6, 7, 8, 9, 10	7Ch
15	CAS Latencies Supported Most Significant Byte (MSB)	High Byte CL Supported = 00h	00h
16	CAS Latency Time, t _{AA} (min)	13.5ns	6Ch
17	Write Recovery Time, t _{WR} (min)	15ns	78h
18	/RAS to /CAS Delay, t _{RCD} (min)	13.5ns	6Ch
19	Minimum Row Active to Row Active Delay Time, t _{RRD} (min)	6ns	30h
20	Minimum Row Precharge Time, t _{RP} (min)	13.5ns	6Ch
21	t _{RAS} and t _{RC} Upper Nibbles	- -	11h
22	Min. Active to Precharge Delay Time, t _{RAS} (min), LSB	36ns	20h
23	Min. Active to Active Refresh Delay Time, t _{RC} (min), LSB	49.5ns	8Ch
24	Min. Refresh Recovery Delay Time, t _{RFC} (min), LSB	110ns	70h
25	Min. Refresh Recovery Time, t _{RFC} (min), MSB	110ns	03h
26	Min. Internal WRITE to READ Command Delay Time, t _{WTR} (min)	7.5ns	3Ch

Serial Presence Detect Information continued on next page.

SERIAL PRESENCE DETECT INFORMATION *(continued)*Serial PD Interface Protocol; I^2C ; Current sink capability of SDA driver $\leq 3mA$; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
27	Min. Internal READ to PRECHARGE Command Delay Time, $t_{RTP}(\text{min})$	7.5ns	3Ch
28	Upper Nibble for t_{FAW}	-	00h
29	Minimum Four Active Window Delay, $t_{FAW}(\text{min})$, LSB	30ns	F0h
30	SDRAM Optional Features	DLL-Off Mode Supporte) RZQ/7 Support	82h
31	SDRAM Thermal and Refresh Options	Non-PARS/ODTS/ASR Extended Temperature Range	01h
32	Module Thermal Sensor	Bit 7=1: Thermal Sensor	80h
33	Module Thermal Heat Spreader Solution	Bit 7=0: Standard Monolithic	00h
34 - 59	-	-	00h
60	Module Nominal Height	29 < Height \leq 30mm	0Fh
61	Module Maximum Thickness	Back: 1 < Thickness \leq 2mm Front: 1 < Thickness \leq 2mm	11h
62	Reference Raw Card Used	Raw Card F, Rev. 00	05h
63	Address Mapping Edge Connector to DRAM	Rank 1: Standard	00h
64 - 116	Reserved	-	00h
117	Module Manufacturer's JEDEC ID Code	STEC	01h
118			A8h
119	Module ID: Module Manufacturing Location	01h = USA 02h = Malaysia	01h/02h
120	Module ID: Module Manufacturing Date		Unique per Build (2 Bytes)
121			
122	Module ID: Module Serial Number		Unique per Build (4 Bytes)
123			
124			
125			
126	Cyclical Redundancy Code		JEDEC Calculation (2 Bytes)
127			

Serial Presence Detect Information continued on next page.

SERIAL PRESENCE DETECT INFORMATION *(continued)*Serial PD Interface Protocol; I²C; Current sink capability of SDA driver ≤ 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
128	Module Part Number	S	53h
129		L	4Ch
130		6	36h
131		4	34h
132		F	46h
133		8	38h
134		W	57h
135		2	32h
136		5	35h
137		6	36h
138		M	4Dh
139		8	38h
140		L	4Ch
141		-	2Dh
142		A	41h
143	1	31h	
144	5	35h	
145	L	4Ch	
146	Module Revision Code		00h
147			00h
148	DRAM Manufacturer's JEDEC ID Code	JEP-106	Varies per DRAM Mfg. (2 Bytes)
149			
150-175	Manufacturer's Specific Data		00h
176-255	Open for Customer Use		00h

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages and temperatures for extended periods may affect device reliability.

Symbol	Parameter	Minimum	Maximum	Units	
V_{DD}	V_{DD} Supply Voltage relative to V_{SS}	-0.4	1.975	V	
V_{DDQ}	V_{DDQ} Supply Voltage relative to V_{SS}	-0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any Pin relative to V_{SS}	-0.4	1.975	V	
I_I	Input Leakage Current; Any input $0V \leq V_{IN} \leq V_{DD}$; V_{REF} Input $0V \leq V_{IN} \leq 0.95V$; (All other pins not under test = $0V$)	Command/Address	-32	32	μA
		/S, CKE, ODT	-16	16	μA
		CK, /CK	-16	16	μA
		DM	-4	4	μA
I_{OZ}	Output Leakage Current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQS and ODT are disabled	-10	10	μA	
I_{VREF}	V_{REF} Leakage Current; V_{REF} = Valid V_{REF} Level	-16	-16	μA	
I_{VTT}	Termination Reference Current from V_{TT}	-600	+600	mA	
V_{TT}	Termination Reference Voltage-Command Address Bus ($\pm 20mV$)	$-0.49 \times V_{DD}$	$+0.50 \times V_{DD}$	V	
T_{STG}	Storage Temperature	-55	100	$^{\circ}C$	
T_C	Operating Temperature-DRAM Components				
	Commercial Operating Temperature	0	85	$^{\circ}C$	
	Industrial Operating Temperature: (W) Option	N/A	N/A	$^{\circ}C$	
T_A	Operating Temperature-Module, Ambient				
	Commercial Operating Temperature	0	70	$^{\circ}C$	
	Industrial Operating Temperature: (W) Option	N/A	N/A	$^{\circ}C$	

Notes:

- Case Temperature, T_C , and Ambient Temperature, T_A , are simultaneous requirements.
- Case Temperature, T_C , is the surface temperature on the center/top side of the DRAM. Please refer to the JESD51.2 Standard for the measurement conditions.
- Case temperature range between $0^{\circ}C$ to $85^{\circ}C$ is the range which all DRAM specifications are supported.
- For case temperature ranges between $85^{\circ}C$ to $95^{\circ}C$, a doubling of the refresh commands in frequency to a 32ms period ($t_{REFI} = 3.9\mu s$) is required. To enter self-refresh mode at this temperature range, an EMRS command is required to change the internal refresh rate.

RECOMMENDED DC OPERATING CONDITIONSAll voltages referenced to V_{SS} .

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1
V_{DDQ}	I/O Supply Voltage	1.425	1.5	1.575	V	4
V_{REF}	I/O Reference Voltage	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2
V_{TT}	I/O Termination Voltage (System)	$V_{REF} - 40$	V_{REF}	$V_{REF} + 40$	mV	3

Notes:

- V_{DD} and V_{DDQ} must track each other. V_{DDQ} must be less than or equal to V_{DD} .
- V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-Peak noise (non-common mode) on V_{REF} may not exceed ± 1 percent of the DC value. Peak-to-Peak AC noise on V_{REF} may not exceed ± 2 percent of $V_{REF}(DC)$. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF} .
- V_{DDQ} tracks with V_{DD} ; V_{DDL} tracks with V_{DD} .

INPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS**INPUT DC LOGIC LEVELS**

Symbol	Parameter	Minimum	Maximum	Units	Notes
$V_{IH}(DC)$	Input High (Logic 1) Voltage	$V_{REF} + 100$	TBD	mV	1
$V_{IL}(DC)$	Input Low (Logic 0) Voltage	-TBD	$V_{REF} - 100$	mV	1
$V_{REFDQ}(DC)$	I/O Reference Voltage (DQ)	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2, 3
$V_{REFCA}(DC)$	I/O Reference Voltage (CMD/ADD)	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2, 3
V_{TT}	Termination Voltage	$V_{DDQ}/2 - TBD$	$V_{DDQ}/2 + TBD$	V	2, 3

INPUT AC LOGIC LEVELS

Symbol	Parameter	Minimum	Maximum	Units	Notes
$V_{IH}(AC)$	Input High (Logic 1) Voltage	$V_{REF} + 175$	-	mV	1, 2
$V_{IL}(AC)$	Input Low (Logic 0) Voltage	-	$V_{REF} - 175$	mV	1, 2

DIFFERENTIAL INPUT LOGIC LEVELS

Symbol	Parameter	Minimum	Maximum	Units	Notes
$V_{IH}diff$	Differential Input High Logic	+200	-	mV	
$V_{IL}diff$	Differential Input Low Logic	-	-200	mV	
V_{IX}	Differential Cross-Point Voltage relative to $V_{DD}/2$	-150	150	mV	

Notes:

- For DQ and DM, $V_{REF} = V_{REFDQ}$. For input only pins except RESET, or $V_{REF} = V_{REFCA}$.
- The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF}(DC)$ by more than $\pm 1\% V_{DD}$ (approximately $\pm 15mV$ for reference).
- Approximately $V_{DD}/2 \pm 15mV$.

OUTPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

AC OUTPUT LEVELS

Symbol	Parameter	Value	Units	Notes
$V_{OH(AC)}$	AC Output High Measurement Level (SR Output)	$V_{TT} + 0.1 \times V_{DDQ}$	V	1
$V_{OL(AC)}$	AC Output Low Measurement Level (SR Output)	$V_{TT} - 0.1 \times V_{DDQ}$	V	1

DC OUTPUT LEVELS

Symbol	Parameter	Value	Units	Notes
$V_{OH(DC)}$	DC Output High Measurement Level (IV Curve Linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OM(DC)}$	DC Output Mid Measurement Level (IV Curve Linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OL(DC)}$	DC Output Low Measurement Level (IV Curve Linearity)	$0.2 \times V_{DDQ}$	V	

DIFFERENTIAL AC and DC OUTPUT PARAMETERS

Symbol	Parameter	Value	Units	Notes
$V_{OHdiff(AC)}$	AC Differential Output High Measurement Level (SR Output)	$+0.2 \times V_{DDQ}$	V	2
$V_{OLdiff(DC)}$	AC Differential Output Low Measurement Level (SR Output)	$-0.2 \times V_{DDQ}$	V	2

Notes:

1. The swing of $\pm 0.1 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 ohms and an effective test load of 25 ohms to $V_{TT} = V_{DDQ}/2$.
2. The swing of $+0.2 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 ohms and an effective test load of 25 ohms to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs.

IDD SPECIFICATIONS AND CONDITIONS

IDD specifications are tested after the device is properly initialized. Recommended Operating Temperature Range. $V_{DD} = +1.5V \pm 0.075V$, $V_{DDQ} = +1.5V \pm 0.075V$, $V_{DDL} = +1.5V \pm 0.075V$, $V_{REF} = V_{DDQ}/2$.

Input slew rate is specified by AC Parametric Test Conditions. IDD parameters are specified with ODT disabled. Data bus consists of DQ, DQS, and /DQS. IDD values must be met with all combinations of EMR bits 10 and 11.

IDDs IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7 are measured as time-averaged currents with all V_{DD} balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.

IDDs IDDQ2NT and IDDQ4R are measured time-averaged currents with all V_{DDQ} balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Note: The user cannot use the IDDQ values to calculate DDR3 SDRAM power directly; the values can only be used to correlate simulated I/O power versus actual I/O power. IDDQ cannot be measured separately since V_{DD} and V_{DDQ} use a merged power layer in the PCB (module) design.

Definitions and parameters for IDD Conditions:

- LOW or 0 (zero) is defined as $V_{IN} \leq V_{IL(AC)}$ (MAX).
- HIGH or 1 (one) is defined as $V_{IN} \geq V_{IH(AC)}$ (MIN).
- STABLE is defined as inputs stable at a HIGH or LOW level.
- FLOATING is defined as inputs at $V_{REF} = V_{DDQ}/2$.
- SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for *address and control signals*; also defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for *DQ signals* not including masks or strobes.
- R_{ON} = RZQ/7 (34 Ohms in MR1).
- R_{TT_NOM} = RZQ/6 (40 Ohms in MR1).
- R_{TT_WR} = RZQ/2 (120 Ohms in MR2).
- Q_{OFF} = Enabled in MR1.
- OTD = Enabled is enabled in MR1 and MR2.
- TDQS = Disabled in MR1.
- External DQ/DQS/DM load resistor is 25 Ohms to $V_{DDQ}/2$.
- Burst Lengths are BL8 fixed.
- AL equals 0 (zero).
- ASR (optional) is disabled.

TIMING PARAMETERS - IDD MEASUREMENTS - CLOCKS

The following table lists the parameters used when measuring the IDD values.

IDD Parameter		DDR3-10600	Units
$t_{CK(MIN)}$		1.5	ns
CL(IDD)		9	t_{CK}
$t_{RCD(MIN)}$		9	t_{CK}
$t_{RC(MIN)}$		33	t_{CK}
$t_{RAS(MIN)}$		24	t_{CK}
$t_{RP(MIN)}$		9	t_{CK}
$t_{FAW(IDD)}$	x4/x8	20	t_{CK}
	x16	N/A	
$t_{RRD(IDD)}$	x4/x8	4	t_{CK}
	x16	N/A	
$t_{RFC(IDD)}$	512Mb	N/A	t_{CK}
	1Gb	74	
	2Gb	N/A	
	4Gb	N/A	

DDR3 IDD SPECIFICATIONS AND CONDITIONS

Symbol	Parameter/Condition
^IDD0	Operating One Bank Active-Precharge Current
	CKE = HIGH; External Clock = ON; $t_{CK}(\text{MIN})$; $t_{RC}(\text{MIN})$; $t_{RAS}(\text{MIN})$; CL(IDD); BL = Note 1; /CS = HIGH between ACTIVATE and PRECHARGE; Command, Address, Bank Address Inputs = SWITCHING with exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Cycling with one bank active at a time; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
^IDD1	Operating One Bank Active-Precharge Current
	CKE = HIGH; External Clock = ON; $t_{CK}(\text{MIN})$; $t_{RC}(\text{MIN})$; $t_{RAS}(\text{MIN})$; CL(IDD); BL = Note 1; /CS = HIGH between ACTIVATE, READ and PRECHARGE; Command Inputs = SWITCHING with exception of ACTIVATE and PRECHARGE commands; Row/Column Addresses = Row Addresses SWITCHING; Address A10 = LOW; Bank Address = Fixed; Data I/O = Read Data: Output Data switches after every clock cycle; Read Data is STABLE during falling DQS; I/O should be FLOATING when no data read; Output Buffer DQ, DQS = OFF; ODT = DISABLED; Active Banks = Bank 0; ACTIVATE to READ to PRECHARGE Loop.
^IDD2N	Precharge Standby Current
	CKE = HIGH; External Clock = ON; $t_{CK} = t_{CK}(\text{MIN})$; /CS = STABLE at 1; All Device Banks = IDLE; Command Inputs = STABLE; Row/Column Addresses = STABLE; Bank Addresses = STABLE; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
^IDD2NT	Precharge Standby ODT Current
	CKE = HIGH; External Clock = ON; $t_{CK}(\text{MIN})$, CL(IDD); BL = Note 1; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = DISABLED; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
^IDDQ2NT	Precharge Standby ODT IDDQ Current (Optional)
	See definition for ^I DD2NT, but measuring IDDQ current rather than IDD current.
^IDD2P₀	Precharge Power-Down Current - Slow Exit
	CKE = HIGH; External Clock = ON; $t_{CK} = t_{CK}(\text{MIN})$, CL(IDD); /CS = STABLE at 1; BL = Note 1; Command, Address, Bank Address Inputs = STABLE at 0; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Precharge Power Down Mode = Slow Exit, See Note 3.
^IDD2P₁	Precharge Power-Down Current - Fast Exit
	CKE = HIGH; External Clock = ON; $t_{CK} = t_{CK}(\text{MIN})$, CL(IDD); /CS = STABLE at 1; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Precharge Power-Down Mode = Fast Exit, See Note 3.

DDR3 IDD Specifications and Conditions continued on next page.

DDR3 IDD SPECIFICATIONS AND CONDITIONS *(continued)*

Symbol	Parameter/Condition
^IDD2Q	Precharge Quiet Standby Current
	CKE = HIGH; External Clock = ON; $t_{CK} = t_{CK(MIN)}$, CL(IDD); /CS = STABLE at 1; Command, Address, Bank Address Inputs = STABLE at 0; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Closed; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0.
^IDD3N	Active Standby Current
	CKE = HIGH; External Clock = ON; $t_{CK} = t_{CK(MIN)}$, CL(IDD); /CS = STABLE at 1; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Open; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
^IDD3P	Active Power-Down Current
	CKE = LOW; External Clock = ON; $t_{CK} = t_{CK(MIN)}$, CL(IDD); BL = Note 1; /CS = STABLE at 1; Command, Address, Bank Address Inputs = STABLE at 0; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = All Banks Open; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0.
^IDD4R	Operating Burst Read Current
	CKE = HIGH; External Clock = ON; $t_{CK} = t_{CK(MIN)}$, CL(IDD); BL = Note 1; /CS = HIGH between READ; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = Read Data Burst (BL8): OUTPUT DATA switches after every clock cycle, read data is STABLE during falling DQS; DM = STABLE at 0; Bank Activity = All Banks open; READ Commands Cycling Through Banks; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
^IDDQ4R	Operating Burst IDDQ Current (Optional)
	See definition for ^I DD4R, but measuring IDDQ current rather than IDD current.
^IDD4W	Operating Burst Write Current
	CKE = HIGH; External Clock = ON; $t_{CK} = t_{CK(MIN)}$, CL(IDD); BL = Note 1; AL = 0; /CS = HIGH between WRITE; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = Write Data Burst (BL8): OUTPUT DATA switches after every clock cycle, read data is STABLE during falling DQS; DM = STABLE at 0; Bank Activity = All Banks Open; Write Commands Cycling Through Banks; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at HIGH; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.
^IDD5B	Burst Refresh Current
	CKE = HIGH; External Clock = ON; $t_{CK} = t_{CK(MIN)}$, $t_{RC} = t_{RC(MIN)}$, CL(IDD), t_{RFC} ; BL = Note 1; AL = 0; /CS = HIGH between REFRESH; Command, Address, Bank Address Inputs = SWITCHING with the exception of ACTIVATE and PRECHARGE commands; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = REFRESH command for every t_{RFC} ; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.

DDR3 IDD Specifications and Conditions continued on next page.

DDR3 IDD SPECIFICATIONS AND CONDITIONS *(continued)*

Symbol	Parameter/Condition
I_{DD6}	Self-Refresh Current - Normal Temperature Range: T_C = 0°C - 85°C
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED, See Note 4; Self-Refresh Temperature Range (SRT) = NORMAL, See Note 5; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD6ET}	Self-Refresh Current - Extended Temperature Range: T_C = 0°C - 95°C (Optional)
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED; Self-Refresh Temperature Range (SRT) = EXTENDED, See Note 4; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Extended Temperature Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD6TC}	Auto Self-Refresh Current - T_C = 0°C - 95°C (Optional)
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; CL(IDD); BL = Note 1; AL = 0; /CS = FLOATING; Auto-Self Refresh (ASR) = DISABLED, See Note 4; Command, Address, Bank Address = FLOATING; Data I/O = FLOATING; DM = STABLE at 0; Bank Activity = Auto Self-Refresh Operation; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = FLOATING.
I_{DD7}	Operating Bank Interleave Read Current
	CKE = HIGH; External Clock = ON; t _{CK} = t _{CK(MIN)} ; t _{RC} = t _{RC(MIN)} ; t _{RAS} = t _{RAS(MIN)} ; t _{RCD} = t _{RCD(MIN)} ; CL(IDD); BL = Note 1; AL = 0; /CS = HIGH between Valid Commands; Row/Column Addresses = STABLE between DESELECTs (DES); Data I/O = Read Data (BL8): Output Data Switches after every Clock Cycle; Read Data is STABLE while DQS is falling; DM = STABLE at 0; Bank Activity = Interleaving Reads Cycling Through Banks; Output Buffer and RTT = Enabled in Mode Registers, See Note 2; ODT Signal = STABLE at 0; Pattern Details = See SDRAM specification Loop Patterns published by supplier/manufacturer.

Notes:

1. BL (Burst Length) = BL8, fixed by MRS; set to MR0 A[1,0] = 00B.
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_WR enable: set MR2 A[10,9] = 10B.
3. Precharge Power Down Mode: set MR0 A12 = 0B for Slow Exit or MR0 A12 = 1B for Fast Exit.
4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature.
5. Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for Normal or 1B for Extended Temperature Range.
6. Refer to SDRAM supplier/manufacturer datasheet and/or DIMM SPD to determine if optional features or requirements are supported by the DDR3 SDRAM device.

MAXIMUM DDR3 IDD VALUES

Notes:

- For a one rank module:
IDD_n is calculated with the rank in IDD_n.
- For two rank modules:
 - IDD0, IDD1, IDD4W, IDD4R, IDD5 and IDD7 are calculated with one rank in IDD_n and one rank in IDD2N **and**
 - IDD2P, IDD2Q, IDD2N, IDD3P, IDD3N and IDD6 are calculated with two ranks in IDD_n.
- For four rank modules:
 - IDD0, IDD1, IDD4W, IDD4R, IDD5 and IDD7 are calculated with one rank in IDD_n and one rank in IDD2N and two ranks in IDD2P, **and**
 - IDD2P, IDD2Q, IDD2N, IDD3P, IDD3N and IDD6 are calculated with two ranks in IDD_n and two ranks in IDD2P.
- Where *n* = corresponding IDD condition listed in the Symbol column.
- Values shown for DDR3 SDRAM components only.
- Values will differ according to the DRAM parts used to manufacture the module.
- IDD values are calculated using worst-case specifications of currently available DRAMs from different manufacturers.
- For Industrial Operating Temperature Range:

When T_C ≤ 0°C:

 - IDD2P and IDD3P must be derated by 4 percent
 - IDD4R and IDD5W must be derated by 2 percent
 - IDD6 and IDD7 must be derated by 7 percent

When T_C ≤ 85°C:

 - IDD0, IDD1, IDD2N, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W and IDD5B must be derated by 2 percent
 - IDD2P must be derated by 20 percent
 - IDD3P must be derated by 30 percent
 - IDD6 must be derated by 80 percent (IDD6 will increase by this amount if T_C < 85°C and the 2x refresh option is still enabled)

Symbol	DDR3-10600	Units
I ^{DD} 0	1,400	mA
I ^{DD} 1	1,560	mA
I ^{DD} 2N	1,040	mA
I ^{DD} 2NT	1,360	mA
I ^{DD} Q2NT	(Optional)	mA
I ^{DD} 2P ₀	224	mA
I ^{DD} 2P ₁	640	mA
I ^{DD} 2Q	960	mA
I ^{DD} 3N	1,040	mA
I ^{DD} 3P	640	mA
I ^{DD} 4R	2,120	mA
I ^{DD} Q4R	(Optional)	mA
I ^{DD} 4W	2,280	mA
I ^{DD} 5B	2,680	mA
I ^{DD} 6	160	mA
I ^{DD} 6 _{ET}	(Optional)	mA
I ^{DD} 6 _{TC}	(Optional)	mA
I ^{DD} 7	4,440	mA

SPEED BINS - DDR3-1333Recommended Operating Temperature Range; $V_{DDQ} = V_{DD} = 1.5V \pm 0.075V$

Symbol	Parameter	Minimum	Maximum	Units	
t_{RCD}	ACT to Internal READ or WRITE Delay Time	13.50	-	ns	
t_{RP}	PRECHARGE Command Period	13.50	-	ns	
t_{RC}	ACT to ACT or REF Command Period	49.50	-	ns	
t_{RAS}	ACT to PRE Command Period	36.00	$9 \times t_{REFI}$	ns	
$t_{CK(avg)}$	CL = 5	CWL = 5	Reserved		ns
		CWL = 6, 7	Reserved		ns
	CL = 6	CWL = 5	2.5	3.3	ns
		CWL = 6	Reserved		ns
		CWL = 7	Reserved		ns
	CL = 7	CWL = 5	Reserved		ns
		CWL = 6	1.875	< 2.5	ns
		CWL = 7	Reserved		ns
	CL = 8	CWL = 5	Reserved		ns
		CWL = 6	1.875	< 2.5	ns
		CWL = 7	Reserved		ns
	CL = 9	CWL = 5, 6	Reserved		ns
		CWL = 7	1.5	< 1.875	ns
	CL = 10	CWL = 5, 6	Reserved		ns
		CWL = 7	1.5	< 1.875	ns
		Supported CL Settings	6, 7, 8, 9, 10		CK
		Supported CWL Settings	5, 6, 7		CK

SPEED BIN NOTES

- The CL and CWL settings result in $t_{CK(AVG).MIN}$ and $t_{CK(AVG).MAX}$ requirements. When selecting a $t_{CK(AVG)}$, both need to be fulfilled.
- $t_{CK(AVG).MIN}$ limits. CAS Latency is not strictly analog; the data and strobe output are synchronized by the DLL. All possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{CK(AVG)}$ value (2.5, 1.875, 1.5 or 1.25 nanoseconds) when calculating $CL [nCK] = t_{AA}[ns]$, rounding up to the next 'supported CL'.
- $t_{CK(AVG).MAX}$ limits: $t_{CK(AVG)} = t_{AA}.MAX / CLSELECTED$, rounding the $t_{CK(AVG)}$ down to the next valid speed bin limit (3.3ns or 2.5ns, or 1.875ns or 1.25ns). This result is $t_{CK(AVG).MAX}$ corresponding to CLSELECTED.
- 'Reserved' settings are not allowed. The user must program a different value.
- 'Optional' settings allow certain devices to support this setting, but it is not a mandatory feature. Refer to the datasheet of the supplier and SPD information to determine if and how this setting is supported.
- Any DDR3 speed bin also supports functional operation at lower frequencies as indicated in the table but are verified by design only and not production tests.
- t_{REFI} is dependent on T_C operating temperature (case temperature).

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS

Clock Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{CKDLL_DIS}	Clock Period Average: DLL Disable Mode	T _C = 0°C to 85°C	8	7,800	ns
		T _C = >85°C to 95°C	8	3,900	ns
t _{CK (AVG)}	Clock Period Average: DLL Enable Mode	See the SPEED BINS Table for the t _{CK} Range.			ns
t _{CH (AVG)}	High Pulse Width Average	-	0.47	0.53	CK
t _{CL (AVG)}	Low Pulse Width Average	-	0.47	0.53	CK
t _{JITPER}	Clock Period Jitter	DLL Locked	-80	80	ps
t _{JITPER, LCK}	Clock Period Jitter	DLL Locking	-70	70	ps
t _{CK (ABS)}	Clock Absolute Period	-	t _{CK(AVG) MIN} + t _{JITPER MIN}	t _{CK(AVG) MAX} + t _{JITPER MAX}	ps
		-			
Clock Jitter					
Symbol	Parameters		Minimum	Maximum	Units
t _{JITCC}	Cycle-to-Cycle Jitter	DLL Locked	160		ps
t _{JITCC, LCK}	Cycle-to-Cycle Jitter	DLL Locking	140		
t _{ERR2PER}	Cumulative Error	2 Cycles	-118	118	ps
t _{ERR3PER}	Cumulative Error	3 Cycles	-140	140	ps
t _{ERR4PER}	Cumulative Error	4 Cycles	-155	155	ps
t _{ERR5PER}	Cumulative Error	5 Cycles	-168	168	ps
t _{ERR6PER}	Cumulative Error	6 Cycles	-177	177	ps
t _{ERR7PER}	Cumulative Error	7 Cycles	-186	186	ps
t _{ERR8PER}	Cumulative Error	8 Cycles	-193	193	ps
t _{ERR9PER}	Cumulative Error	9 Cycles	-200	200	ps
t _{ERR10PER}	Cumulative Error	10 Cycles	-205	205	ps
t _{ERR11PER}	Cumulative Error	11 Cycles	-210	210	ps
t _{ERR12PER}	Cumulative Error	12 Cycles	-215	215	ps
t _{ERR_nPER}	n = 13, 14...49, 50	n Cycles	t _{ERR_nPER MIN} = (1 + 0.68ln[n]) x t _{JITPER MIN}	t _{ERR_nPER MAX} = (1 + 0.68ln[n]) x t _{JITPER MAX}	ps
DQ Input Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{DSAC175}	Data Setup Time to DQS, /DQS	Base (Specification)	-	-	ps
		VREF @ 1 V/ns	-	-	
t _{DHAC175}	Data Hold Time from DQS, /DQS	Base (Specification)	65	-	ps
		VREF @ 1 V/ns	165	-	
t _{DSAC150}	Data Setup Time to DQS, /DQS	Base (Specification)	30	-	ps
		VREF @ 1 V/ns	180	-	
t _{DHAC150}	Data Hold Time from DQS, /DQS	Base (Specification)	65	-	ps
		VREF @ 1 V/ns	165	-	
t _{DIPW}	Minimum Data Pulse Width	-	400	-	ps

AC Operating Conditions and Electrical Parameters continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS (Continued)

DQ Output Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{DQSQ}	DQS, /DQS to DQ Skew	Per Access	-	125	ps
t _{QH}	DQ Output Hold Time from DQS, /DQS	-	0.38	-	ps
t _{LZ (DQ)}	DQ Low-Z Time from CK, /CK	-	-500	250	ps
t _{HZ (DQ)}	DQ High-Z Time from CK, /CK	-	-	250	ps
DQ Strobe Input Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{DQSS}	DQS, /DQS Rising to CK, /CK Rising		-0.25	0.25	CK
t _{DQSL}	DQS, /DQS Differential Input Low Pulse Width		0.45	0.55	CK
t _{DQSH}	DQS, /DQS Differential Input High Pulse Width		0.45	0.55	CK
t _{DSS}	DQS, /DQS Falling Setup to CK, /CK Rising		0.2	-	CK
t _{DSH}	DQS, /DQS Falling Hold from CK, /CK Rising		0.2	-	CK
t _{WPRE}	DQS, /DQS Differential WRITE Preamble		0.9	-	CK
t _{WPST}	DQS, /DQS Differential WRITE Postamble		0.3	-	CK
DQ Strobe Output Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{DQSCK}	DQS, /DQS Rising To/From Rising CK, /CK		-255	255	ps
t _{DQSKDLL_DIS}	DQS, /DQS Rising To/From Rising CK, /CK when DLL is disabled.		1	10	ns
t _{QSH}	DQS, /DQS Differential Output High Time		0.40	-	CK
t _{QSL}	DQS, /DQS Differential Output Low Time		0.40	-	CK
t _{LZ (DQS)}	DQS, /DQS Low-Z Time (RL - 1)		-500	250	ps
t _{HZ (DQS)}	DQS, /DQS High-Z Time (RL + BL/2)		-	250	ps
t _{RPRE}	DQS, /DQS Differential READ Preamble		0.9	-	CK
t _{RPST}	DQS, /DQS Differential READ Postamble		0.3	-	CK
Command and Address Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{DLLK}	DLL Locking Time		-	512	CK
t _{ISAC175}	CTRL, CMD, ADDR Setup to CK, /CK	Base (Specification)	65	-	ps
		VREF @ 1 V/ns	240	-	ps
t _{IH}	CTRL, CMD, ADDR Hold from CK, /CK	Base (Specification)	190	-	ps
		VREF @ 1 V/ns	340	-	ps
t _{ISAC150}	CTRL, CMD, ADDR Setup to CK, /CK	Base (Specification)	140	-	ps
		VREF @ 1 V/ns	240	-	ps
t _{IPW}	CTRL, CMD, ADDR Minimum Pulse Width		620	-	ps
t _{RCD}	ACTIVATE to Internal READ or WRITE Delay		See the Speed Bins Table for t _{RCD} .		ns
t _{RP}	PRECHARGE Command Period		See the Speed Bins Table for t _{RP} .		ns
t _{RAS}	ACTIVATE-to-PRECHARGE Command Period		See the Speed Bins Table for t _{RAS} .		ns
t _{RC}	ACTIVATE-to-ACTIVATE Command Period		See the Speed Bins Table for t _{RC} .		ns
t _{RRD}	ACTIVATE-to-ACTIVATE Minimum Command Period	1KB Page Size	MIN = > of 4CK or 6ns		CK
		2KB Page Size	MIN = > of 4CK or 7.5ns		CK

AC Operating Conditions and Electrical Parameters continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS (Continued)

Command and Address Timing (continued)					
Symbol	Parameters		Minimum	Maximum	Units
t _{FAW}	Four ACTIVATE Windows	1 KB Page Size	30	-	ns
		2 KB Page Size	45	-	ns
t _{WR}	Write Recovery Time	-	15ns	-	ns
t _{WTR}	Delay from Start of Internal WRITE Transaction to Internal READ Command		> of 4CK or 7.5ns	-	CK
t _{RTP}	READ-to-PRECHARGE Time		> of 4CK or 7.5ns	-	CK
t _{CCD}	/CAS-to/CAS Command Delay		4CK	-	CK
t _{DAL}	Auto Precharge Write Recovery + Precharge Time		WR + t _{RP} /t _{CK} (AVG)	-	CK
t _{MRD}	MODE REGISTER SET Command Cycle Time		4CK	-	CK
t _{MOD}	MODE REGISTER SET Command Update Delay		> of 12CK or 15ns	-	CK
t _{MPRR}	MULTIPURPOSE REGISTER READ Burst End to Mode Register Set for Multipurpose Register Exit		1CK	-	CK
Calibration Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{ZQINIT}	ZQCL Command: Long Calibration Time	POWER-UP and RESET	512	-	CK
t _{ZQOPER}	ZQCL Command: Short Calibration Time	Normal Operation	256	-	CK
t _{ZQCS}	ZQCS Command: Short Calibration Time		64	-	CK
Initialization and Reset Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{XPR}	Exit Reset from CKE HIGH to a Valid Command		> of 5CK or t _{RFC} + 10ns	-	CK
t _{VDDPR}	Power Supply Ramp to Power Supplies Stable		-	200	ms
t _{RPS}	/RESET LOW to Power Supplies Stable		0	200	ms
t _{IOz}	/RESET LOW to I/O and RTT High-Z		-	20	ns
Refresh Timing					
Symbol	Parameters		Minimum	Maximum	Units
t _{RFC}	REFRESH-to-ACTIVATE or REFRESH Command Period		110	9 x t _{REFI}	ns
	Maximum Refresh Period	T _C = 0°C to 85°C	64 (1X)		ms
		T _C = > 85°C to 95°C	32 (2X)		ms
t _{REFI}	Maximum Average Periodic Refresh	T _C = 0°C to 85°C	7.8 (64ms/8,192)		μs
		T _C = > 85°C to 95°C	3.9 (32ms/8,192)		μs

AC Operating Conditions and Electrical Parameters continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS (Continued)

Self-Refresh Timing					
Symbol	Parameters	Minimum	Maximum	Units	
t _{XS}	Exit Self-Refresh to commands not requiring a locked DLL	> of 5CK or t _{RFC} + 10ns	-	CK	
t _{XDLL}	Exit Self-Refresh to commands that require a locked DLL	t _{DLLK} (MIN)	-	CK	
t _{CKESR}	Minimum CKE Low Pulse Width for Self-Refresh Entry to Self-Refresh Exit Timing	t _{CKE} (MIN) + CK	-	CK	
t _{CKSRE}	Valid Clocks after Self-Refresh Entry or Power-Down Entry	> of 5CK or 10ns	-	CK	
t _{CKSRX}	Valid Clocks b/f Self-Refresh Exit, Power-Down Exit, or Reset Exit	> of 5CK or 10ns	-	CK	
Power-Down Timing					
Symbol	Parameters	Minimum	Maximum	Units	
t _{CKE}	CKE MIN Pulse Width	> of 3CK or 5.625ns		CK	
t _{CPDED}	Command Pass Disable Delay	1	N/A	CK	
t _{PD}	Power-Down Entry to Power-Down Exit Timing	t _{CKE} (MIN)	9 x t _{REFI}	CK	
t _{ANPD}	Begin Power-Down Period prior to CKE Registered HIGH	WL - 1CK		CK	
PDE	Power-Down Entry Period; ODT synchronous/asynchronous	> of t _{ANPD} or t _{RFC} - REFRESH Command to CKE LOW Time		CK	
PDX	Power-Down Exit Period; ODT synchronous/asynchronous	t _{ANPD} + t _{XPDLL}		CK	
Power-Down Entry Minimum Timing					
Symbol	Parameters	Minimum	Maximum	Units	
t _{ACTPDEN}	ACTIVATE Command to Power-Down Entry	1	-	CK	
t _{PRPDEN}	PRECHARGE/PRECHARGE ALL Command to Power-Down Entry	1	-	CK	
t _{REFPDEN}	REFRESH Command to Power-Down Entry	1	-	CK	
t _{MRSPDEN}	MRS Command to Power-Down Entry	t _{MOD} (MIN)	-	CK	
t _{RDPDEN}	READ/READ with Auto-Precharge Command to Power-Down Entry	RL + 4 + 1	-	CK	
t _{WRPDEN}	WRITE Command to Power-Down Entry	BL8 (OTF, MRS) BC4OTF	WL + 4 + t _{WR} /t _{CK} (AVG)	-	CK
		BC4MRS	WL + 2 + t _{WR} /t _{CK} (AVG)	-	
t _{WRAPDEN}	WRITE with Auto-Precharge Command to Power-Down Entry	BL8 (OTF, MRS) BC4OTF	WL + 4 + WR + 1	-	CK
		BC4MRS	WL + 2 + WR + 1		
Power-Down Exit Timing					
Symbol	Parameters	Minimum	Maximum	Units	
t _{XP}	DLL ON, any valid command, or DLL OFF to commands not requiring a locked DLL	> of 3CK or 6ns	-	CK	
t _{XPDLL}	Precharge Power-Down with DLL OFF to commands that require a locked DLL	> of 10CK or 24ns	-	CK	

AC Operating Conditions and Electrical Parameters continued on next page.

AC OPERATING CONDITIONS AND ELECTRICAL PARAMETERS (Continued)

ODT Timing				
Symbol	Parameters	Minimum	Maximum	Units
ODTL ON	RTT Synchronous Turn-On Delay	CWL + AL - 2CK		CK
ODTL OFF	RTT Synchronous Turn-Off Delay	CWL + AL - 2CK		CK
t _{AON}	RTT Turn-On from ODTL On Reference	-250	250	ps
t _{AOFF}	RTT Turn-Off from ODTL Off Reference	0.3	0.7	CK
t _{AONPD}	Asynchronous RTT Turn-On Delay (Power-Down with DLL OFF)	2	8.5	ns
t _{AOFPD}	Asynchronous RTT Turn-Off Delay (Power-Down with DLL OFF)	2	7.5	ns
ODTH8	ODT HIGH Time with WRITE Command and BL8	6	-	CK
ODTH4	ODT HIGH Time without WRITE Command or with WRITE Command with BC4	4	-	CK
Dynamic ODT Timing				
Symbol	Parameters	Minimum	Maximum	Units
ODTLCNW	RTT_NOM-to-RTT_WR Change Skew	WL - 2CK		CK
ODTLCNW4	RTT_NOM-to-RTT_WR Change Skew	BC4	4CK + ODTL Off	CK
ODTLCNW8	RTT_NOM-to-RTT_WR Change Skew	BL8	6CK + ODTL Off	CK
t _{ADC}	RTT Dynamic Change Skew	0.3	0.7	CK
Write-Leveling Timing				
Symbol	Parameters	Minimum	Maximum	Units
t _{WLMRD}	First DQS, /DQS Rising Edge	40	-	CK
t _{WLDQSEN}	DQS, /DQS Delay	25	-	CK
t _{WLS}	Write-Leveling Setup from rising CK, /CK crossing to rising DQS, /DQS crossing	195	-	ps
t _{WLH}	Write-Leveling Hold from rising DQS, /DQS crossing to rising CK, /CK crossing	195	-	ps
t _{WLO}	Write-Leveling Output Delay	0	9	ns
t _{WLOE}	Write-Leveling Output Error	0	2	ns

Notes:

1. It is recommended that the system designer or system engineer reference the latest specification release notes from the DRAM manufacturers in regards to these signals. The default operational characteristics are listed here for reference only.

REVISION HISTORY

Revision	Date	Description
-101	06/28/2007	Initial release.
-102	05/24/2008	PCB updated to planar. SPD corrected.
-103	07/09/2009	Revised to R/C F and updated to current specifications. Preliminary notice removed.
-104	07/13/2009	Dimensions and Block Diagram illustrations update to show combo SPD/TS.
-105	10/12/2009	SPD/TS move to front of PCB. T _A updated and Note 1 added. Duplicate termination on clock corrected. SPD Byte 31-34 corrected.

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