

32M X 32 Bits (128MB) 144-Pin SDRAM SO-DIMM (PC100)

FEATURES

- PC100 Compliant
(see *Ordering Information* for options)
- Burst Mode Operation
- Auto and self refresh capability
(8192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V \pm 0.3V power supply
- MRS cycle with address key programs
 - Latency (access from column address)
 - Burst Length (1, 2, 4, 8, and full page)
 - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM

GENERAL DESCRIPTION

The SL32G8F32M8G-A10xV(U) is a 32M x 32 bits Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of four CMOS 8M x 8 bit x 4 bank SDRAMs in 54-pin 400-mil TSOP II packages mounted on a 144-pin glass epoxy substrate. A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1 μ F are mounted for the SDRAMs and the EEPROM. Damping resistors are mounted for the data lines.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

See *Ordering Information* for PC100 performance options.

PIN CONFIGURATION

Pin Symbols

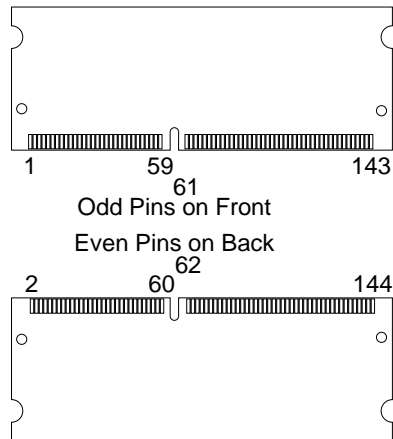
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	21	VSS	41	DQ10	61	CLK0	81	VDD	101	VDD	121	DQ24	141	SDA
2	VSS	22	VSS	42	DQ42*	62	CKE0	82	VDD	102	VDD	122	DQ56*	142	SCL
3	DQ0	23	DQMB0	43	DQ11	63	VDD	83	DQ16	103	A6	123	DQ25	143	VDD
4	DQ32*	24	DQMB4*	44	DQ43*	64	VDD	84	DQ48*	104	A7	124	DQ57*	144	VDD
5	DQ1	25	DQMB1	45	VDD	65	$\overline{\text{RAS}}$	85	DQ17	105	A8	125	DQ26		
6	DQ33*	26	DQMB5*	46	VDD	66	$\overline{\text{CAS}}$	86	DQ49*	106	BA0	126	DQ58*		
7	DQ2	27	VDD	47	DQ12	67	$\overline{\text{WE}}$	87	DQ18	107	VSS	127	DQ27		
8	DQ34*	28	VDD	48	DQ44*	68	CKE1*	88	DQ50*	108	VSS	128	DQ59*		
9	DQ3	29	A0	49	DQ13	69	$\overline{\text{S}}_0$	89	DQ19	109	A9	129	VDD		
10	DQ35*	30	A3	50	DQ45*	70	A12	90	DQ51*	110	BA1	130	VDD		
11	VDD	31	A1	51	DQ14	71	$\overline{\text{S}}_1^*$	91	VSS	111	A10/AP	131	DQ28		
12	VDD	32	A4	52	DQ46*	72	A13*	92	VSS	112	A11	132	DQ60*		
13	DQ4	33	A2	53	DQ15	73	NC	93	DQ20	113	VDD	133	DQ29		
14	DQ36*	34	A5	54	DQ47*	74	CLK1	94	DQ52*	114	VDD	134	DQ61*		
15	DQ5	35	VSS	55	VSS	75	VSS	95	DQ21	115	DQMB2	135	DQ30		
16	DQ37*	36	VSS	56	VSS	76	VSS	96	DQ53*	116	DQMB6*	136	DQ62*		
17	DQ6	37	DQ8	57	NC	77	NC	97	DQ22	117	DQMB3	137	DQ31		
18	DQ38*	38	DQ40*	58	NC	78	NC	98	DQ54*	118	DQMB7*	138	DQ63*		
19	DQ7	39	DQ9	59	NC	79	NC	99	DQ23	119	VSS	139	VSS		
20	DQ39*	40	DQ41*	60	NC	80	NC	100	DQ55*	120	VSS	140	VSS		

* Not used

(continued on the next page)

PIN CONFIGURATION *(continued)*

Pin Arrangement



Pin Functions

Pin Name	Pin Function
A0-A10/AP, A11-A12	Address Inputs (multiplexed)
BA0, BA1	Select Bank
DQ0-DQ31	Data In/Out
\overline{WE}	Read/Write Enable
CLK0, CLK1	Clock Input
CKE0	Clock Enable Input
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
DQMB0-DQMB3	Data Input/Output Mask
$\overline{S_0}$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

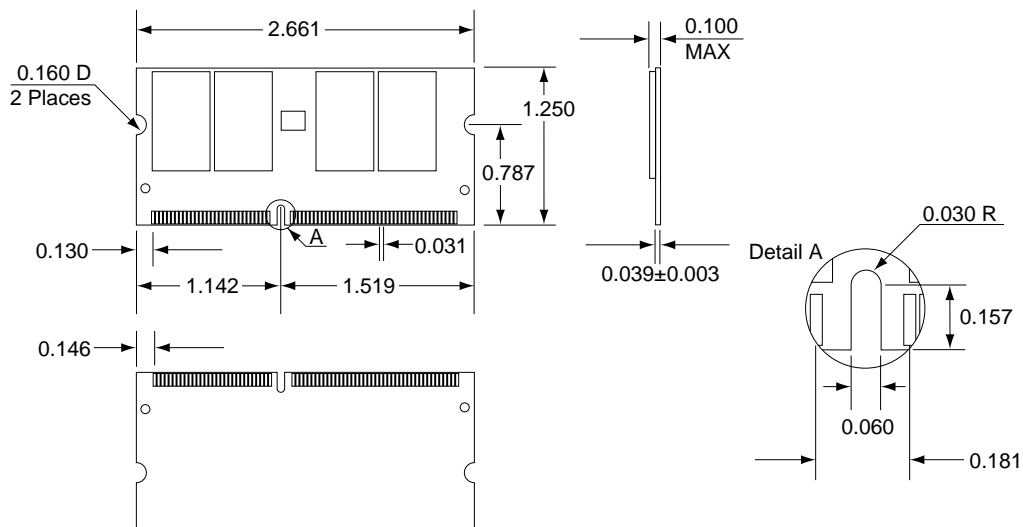
ORDERING INFORMATION

Part Number	PC100 100MHz Parameters					
	CL	t _{RCD}	t _{RP}	t _{RC}	Units	Comment
SL32G8F32M8G-A10AV(U)	3	3	3	8	clks	slowest supported (option "A")
N/A	3	2	3	8	clks	2nd choice (option "B")
SL32G8F32M8G-A10CV(U)	3	2	2	7	clks	target (option "C")
SL32G8F32M8G-A10DV(U)	2	2	2	7	clks	goal (option "D")

Note: U added to part number selects the RoHS compliant lead free version

PACKAGE DIMENSIONS

Units: Inches



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

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SERIAL PRESENCE DETECT INFORMATION

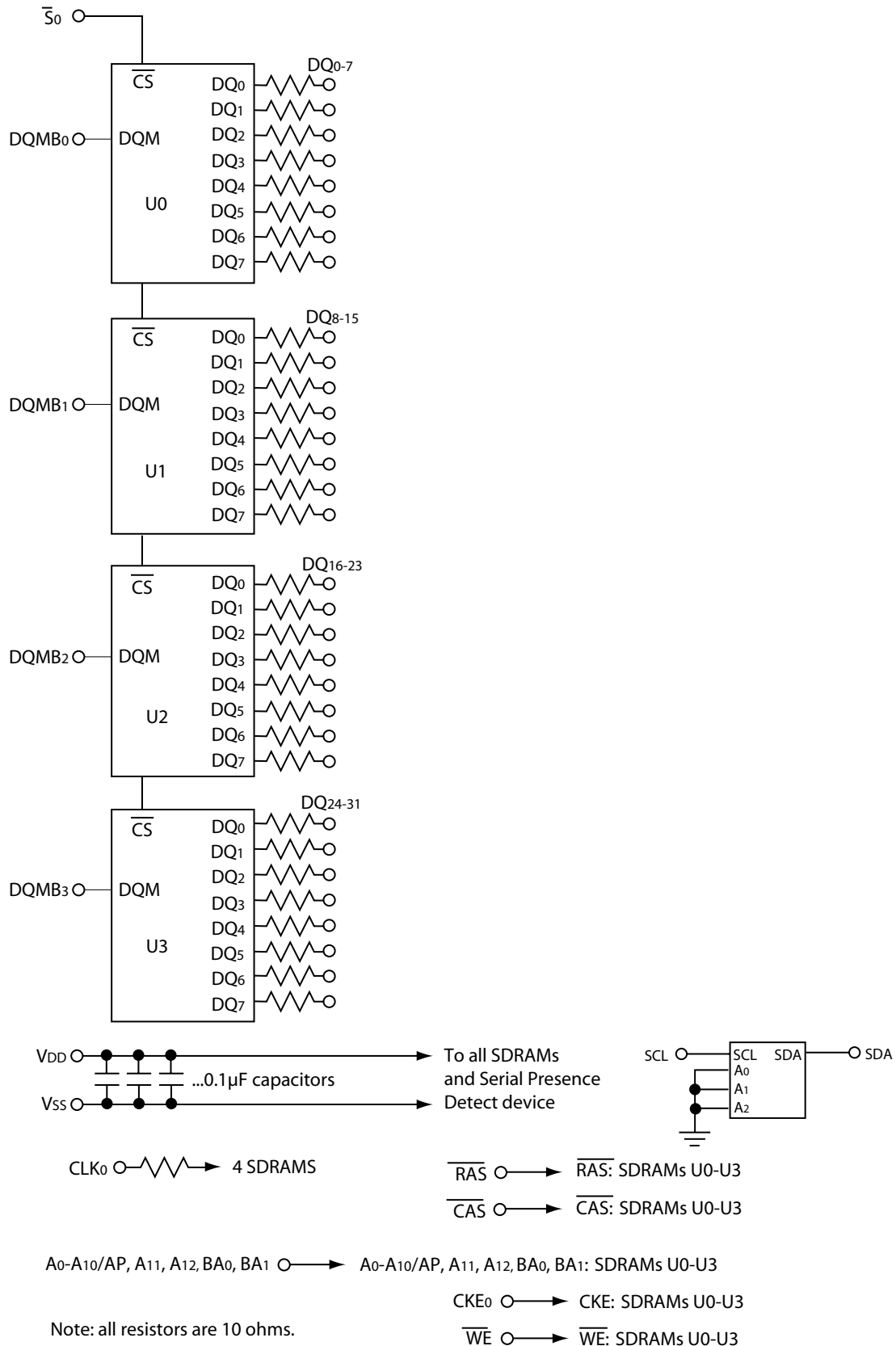
Serial PD Interface Protocol: I²C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported				Hex Value			
		A	B	C	D	A	B	C	D
0	# of bytes written into serial memory at module manufacturer	128 bytes				80h			
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)				08h			
2	Fundamental memory type	SDRAM				04h			
3	# of row addresses on this assembly	13				0Dh			
4	# of column addresses on this assembly	10				0Ah			
5	# of module banks on this assembly	1 bank				01h			
6	Data width of this assembly	32 bits				20h			
7	...Data width of this assembly (continued)	—				00h			
8	Voltage interface standard of this assembly	LVTTL				01h			
9	SDRAM cycle time at CL=3 (tCYC)	10ns	—	10ns	10ns	A0h	—	A0h	A0h
10	SDRAM access time from clock at CL=3 (tAC)	6ns	—	6ns	6ns	60h	—	60h	60h
11	DIMM configuration type	None				00h			
12	Refresh rate/type	7.8µs, Self-refresh				82h			
13	SDRAM width	8 bits				08h			
14	Error Checking DRAM data width	0 bits				00h			
15	Min. CLK delay for back-to-back rand. col. addr.	tCCD=1 CLK				01h			
16	SDRAM device attributes: burst lengths supported	1,2,4, 8, and Full Page				8Fh			
17	SDRAM device attributes: # of banks on SDRAM device	4 banks				04h			
18	SDRAM device attributes: CAS latency	CAS latency = 2,3				06h			
19	SDRAM device attributes: CS latency	CS latency = 0				01h			
20	SDRAM device attributes: Write latency	Write Latency = 0				01h			
21	SDRAM module attributes	non-buff., non-reg.				00h			
22	SDRAM device attributes: general	VCC10%, B/R, S/W, P/A, A/P				0Eh			
23	Minimum clock cycle time at CL=2 (tCYC)	12ns	—	15ns	10ns	C0h	—	F0h	A0h
24	Max. data access time form clock at CL=2 (tAC)	8ns	—	8ns	6ns	80h	—	80h	60h
25	Minimum clock cycle time at CL=1 (tCYC)	—	—	—	—	—	—	00h	00h
26	Max. data access time from clock at CL=1 (tAC)	—	—	—	—	—	—	00h	00h
27	Minimum row precharge time (tRP)	20ns	—	20ns	20ns	14h	—	14h	14h
28	Minimum row active to row active delay (tRRD)	20ns	—	20ns	20ns	14h	—	14h	14h
29	Minumum RAS to CAS (tRCD)	20ns	—	20ns	20ns	14h	—	14h	14h
30	Minumum RAS pulse width (tRAS)	50ns	—	50ns	50ns	32h	—	32h	32h
31	Module bank density	128MB				20h			
32	Min. command and address signal setup time (tAS)	2ns				20h			
33	Min. command and address signal hold time (tAH)	1ns				10h			
34	Min. data signal input setup time (tDS)	2ns				20h			

continued on the next page

Byte #	Function Described	Function Supported				Hex Value			
		A	B	C	D	A	B	C	D
35	Min. data signal input hold time (t _{DH})	1ns				10h			
36-61	Superset information (may be used in future)	—				00h			
62	SPD revision	1.2	—	1.2	1.2	12h	—	12h	12h
63	Checksum for bytes 0-62	JEDEC calculation				xxh			
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code				7Fh			
65	Man. JEDEC ID code (continued)	STEC's ID				A8h			
66-71						00h			
72	Manufacturing location	STEC USA or STEC Malaysia				01h (USA) or 02h			
73-90	Manufacturer's part number					xxh			
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)				01h			
92						00h			
93	Manufacturing date	Year (BCD)				yy			
94		Calender Week (BCD)				w w			
95	Assembly serial number	Tester number				ss			
96		Serial number (bits 7-0)				ss			
97		Serial number (bits 15-8)				ss			
98		Serial number (bits 23-16)				ss			
99-125	Manufacturer's specific data					xxh			
126	Intel specification frequency	100MHz				64h			
127	Intel specification details	Detailed 100MHz Info				8Fh	—	8Fh	8Fh

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to VSS	V _{IN} , V _{OUT}	-1.0 to +4.6	V
Voltage on VCC Supply Relative to VSS	V _{DD}	-1.0 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	4	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to VSS, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V _{DD}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	0	0.8	V	2
Output High Voltage Level	V _{OH}	2.4	—	—	V	I _{OH} =-2mA
Output Low Voltage Level	V _{OL}	—	—	0.4	V	I _{OL} =2mA
Input Leakage Current	I _{IL}	-40	—	40	μA	3
Output Leakage Current	I _{OL}	-10	—	10	μA	4

Notes:

- V_{IH}(max)=5.6 V AC (pulse width <=3 ns acceptable)
- V_{IL}(min) = -2.0V AC (pulse width <=3 ns acceptable)
- Any input 0<=V_{IN}<=V_{DD}+0.3V, all other pins not under test = 0 V.
- Data out is disabled, 0<=V_{OUT}<=V_{DD}

CAPACITANCE (T_A=23 °C, f=1MHz)

Item	Symbol	Max	Units
Input Capacitance (A ₀ -A ₁₀ /AP, A ₁₁ -12, BA ₀ , BA ₁)	C _{IN1}	30	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	30	pF
Input Capacitance (CLK ₀ , CLK ₁)	C _{IN3}	13	pF
Input Capacitance (CKE ₀)	C _{IN4}	30	pF
Input Capacitance ($\overline{\text{S}}_0$)	C _{IN5}	30	pF
Input Capacitance (DQMB ₀ -DQMB ₃)	C _{IN6}	15	pF
Input/Output Capacitance (DQ ₀ -DQ ₃₁)	C _{IO1}	16.5	pF

*(Where U selects the RoHS Compliant, lead-free version)***DC CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted. TA=0 to 70°C)

Parameter	Symbol	Test Condition	Max	Units
Operating Current (One Bank Active)	ICC1S	Burst length=1, tRC>=tRC(min), IOL=0mA, Outputs open	400	mA
Precharge Standby Current in Power-Down Mode	ICC2P	CKE<=VIL(max), tCLK=10ns,	8	mA
	ICC2PS	CKE and CLK<=VIL(max), tCLK=infinity	8	mA
Precharge Standby Current in Non Power-Down Mode	ICC2N	CKE and S>=VIH(min), tCLK=10ns Input signals are changed one time during 20ns	80	mA
	ICC2NS	CKE>=VIH(min), CLK<=VIL(max), tCLK= infinity Input signals are stable	40	mA
Active Standby Current in Power-Down Mode	ICC3P	CKE<=VIL(max), tCLK=10ns	48	mA
	ICC3PS	CKE and CLK<=VIL(max), tCLK=infinity	48	mA
Active Standby Current in Non Power-Down Mode (One Bank Active)	ICC3N	CKEand S>=VIH(min), tCLK=10ns, Input signals are changed one time during 20ns	120	mA
	ICC3NS	CKE>=VIH(min), CLK<=VIL(max), tCLK=infinity Inputs are stable	100	mA
Operating Current (Burst Mode)	ICC4	IOL=0mA, Page Burst, ICCD=2 CLKs, Outputs open 4 banks activated	440	mA
Refresh Current (Refresh Period is 64ms)	ICC5	tRC>=tRC(min)	760	mA
Self Refresh Current	ICC6	CKE<=0.2V	12	mA

AC TIMING PARAMETERS

(AC operating conditions unless otherwise noted. Refer to the individual component, not the whole module.)

Parameter	Symbol	CL2		CL3		Unit	Notes
		Min	Max	Min	Max		
Clock Period	Option A Option C Option D	t _{CYC}	12 15 10		10 10 10	ns	
Clock High Time		t _{CH}	2.5		2.5	ns	1
Clock Low Time		t _{CL}	2.5		2.5	ns	
Input Setup Times		t _{SI}	2		2	ns	
Input Hold Times		t _{HI}	1		1	ns	
Output Valid From Clock	Option A Option C Option D	t _{AC}		8 8 6		6 6 6	ns 2
Output Hold From Clock		t _{OH}	3		3	ns	3
Output Valid to Z		t _{OHZ}	3	9	3	9	ns
CAS to CAS Delay		t _{CCD}	1		1	t _{CLK}	
CAS Bank Delay		t _{CBD}	1		1	t _{CLK}	
CKE to Clock Disable		t _{CKE}	1		1	t _{CLK}	
RAS Precharge Time		t _{RP}	20		20	ns	
RAS Active Time		t _{RAS}	50		50	ns	
Active to Command Delay (RAS to CAS Delay)		t _{RCD}	20		20	ns	
RAS to RAS Bank Activate Delay		t _{RRD}	20		20	ns	
RAS Cycle Time	Option A Option C Option D	t _{RC}	80 70 70		80 70 70	ns	
DQM to Input Data Delay		t _{DQD}	0		0	t _{CLK}	
Write Cmd. to Input Data Delay		t _{DWD}	0		0	t _{CLK}	
Mode Register set to Active Delay		t _{MRD}	2		2	t _{CLK}	
Precharge to O/P in High-Z		t _{ROH}	CL		CL	t _{CLK}	
DQM to Data in HiZ for Read		t _{DQZ}	2		2	t _{CLK}	
DQM to Data Mask for Write		t _{DQM}	0		0	t _{CLK}	4
Data-In to PRE Command Period		t _{DPL}	2		2	t _{CLK}	
Data-In to ACT (PRE) Command Period (Auto Precharge)		t _{DAL}	5		5	t _{CLK}	
Power Down Mode Entry		t _{SB}		1		1	t _{CLK}
Self Refresh Exit Time		t _{XSR}	1		1	t _{CLK}	
Power Down Exit Setup Time		t _{PED}	75		75	ns	5
Clock Stop During Self Refresh or Power Down		t _{CLKSTP}	200		200	t _{CLK}	6

Notes:

1. Rated @ 1.5V
2. LVTTTL levels, rated @ 50pF, all outputs switching, 5.2ns @ 0pF
3. 3ns @ 50pF, need 1.8ns @0pF
4. Data Masked on the same clock.
5. Timing is asynchronous. If t_{SET} is not met by rising edge of CLK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or powerdown, 200 clocks are required before CKE is high.

AC TIMING PARAMETERS *(continued)*

Notes:

1. Rated @ 1.5V
2. Limited application, 2 banks, all outputs switching
3. LVTTTL levels, rated @ 50pF, all outputs switching, 5.2ns @ 0pF
4. 3ns @ 50pF, need 1.8ns @0pF
5. $t_{RP}=2$ a SPD Option
6. $t_{RCD}=2$ a SPD Option
7. 7 clks for $t_{RP}=2$
8. Data Masked on the same clock.
9. Timing is asynchronous. If t_{SET} is not met by rising edge of CLK then CKE is assumed latched on next cycle.
10. If the clock is stopped during self refresh or powerdown, 200 clocks are required before CKE is high.

AC OPERATING TEST CONDITIONS

($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value
AC input levels	$V_{IH}/V_{IL}=2.4V/0.4V$
Input timing measurement ref. level	1.4V
Input rise and fall time	$t_r/t_f=1ns/1ns$
Output measurement reference level	1.4V
Output load condition	See Figure 2.

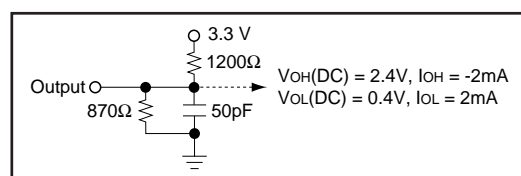


Figure 1. DC Output Load Circuit

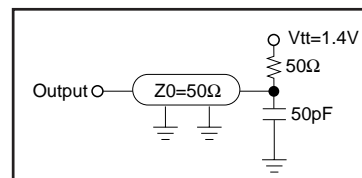


Figure 2. AC Output Load Circuit

REVISION HISTORY

Rev. **Change Description from Previous Revision**

- 101 09/01/2001. Initial release.
- 102 08/07/2007. Logo updated. New document part number assigned to separate product Rev. C (61000-02002-xxx) from product Rev A (this document).
- 103 08/17/2007. Reverted spec data to cover A and C option speeds.