

FEATURES

- PC133 Compliant
(Option A: tCYC = 7.5ns@CL = 3)
(Option D: tCYC = 7.5ns@CL = 2, 3)
- Burst Mode Operation
- Auto and self refresh capability
(8,192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- MRS cycle with address key programs
 - Latency (access from column address)
 - Burst Length (1, 2, 4, 8, and full page)
 - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- RoHS Compliant, Pb-free (lead-free)

GENERAL DESCRIPTION

The SLx64G6F32M8G-A75zVU is a 32M x 64 bit Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of eight 4M x 16 bit x 4 bank SDRAMs in 54-pin 400-mil TSOP II lead-free packages mounted on a 144-pin glass epoxy substrate. The SDRAMs are organized into 2 ranks.

A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1µF are mounted. Damping resistors are mounted for the data lines.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

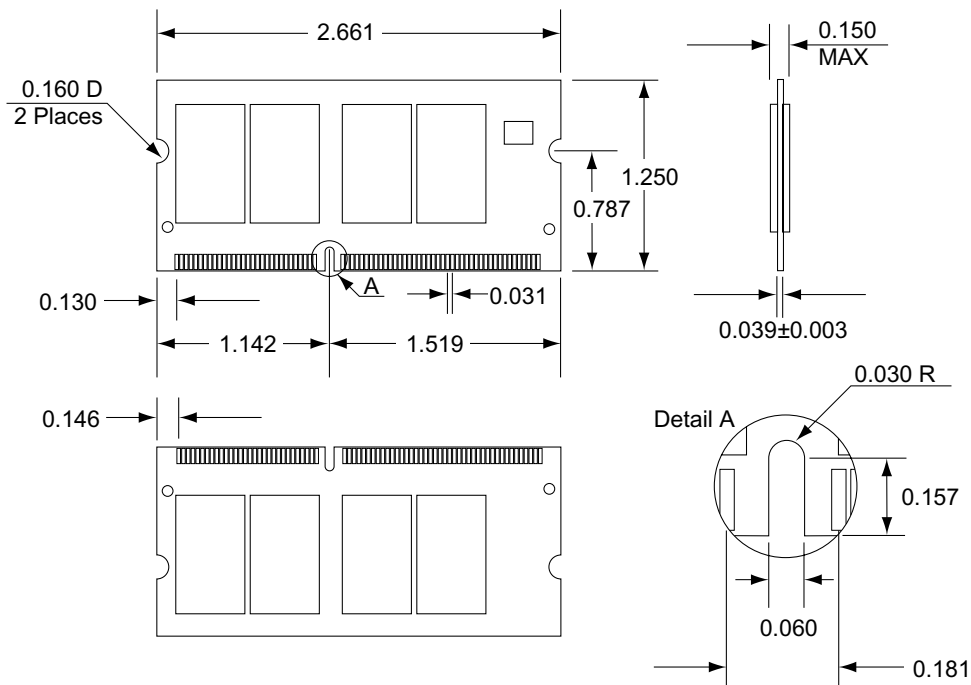
See *Ordering Information* for PC133 performance options.

ORDERING INFORMATION

Part Number	DRAM	PC133 133MHz Parameters				
		CL	tRCD	tRP	tRC	Comment
SLS64G6F32M8G-A75AVU	Samsung	3 clks	20ns	20ns	66ns	Refer to Option A in this specification.
SLS64G6F32M8G-A75DVU	Samsung	2 clks	15ns	15ns	60ns	Refer to Option D in this specification.
SLQ64G6F32M8G-A75AVU	Qimonda	3 clks	20ns	20ns	66ns	Refer to Option A in this specification.
SLQ64G6F32M8G-A75DVU	Qimonda	2 clks	15ns	15ns	60ns	Refer to Option D in this specification.

PACKAGE DIMENSIONS

Units are in inches. Tolerances are ±0.005 unless otherwise specified.



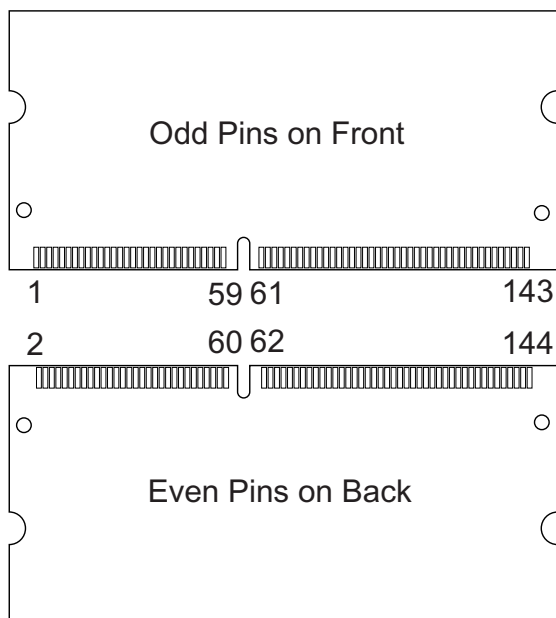
PIN CONFIGURATION

Pin Symbols (* = Not Used)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	21	VSS	41	DQ10	61	CLK0	81	VDD	101	VDD	121	DQ24	141	SDA
2	VSS	22	VSS	42	DQ42	62	CKE0	82	VDD	102	VDD	122	DQ56	142	SCL
3	DQ0	23	DQMB0	43	DQ11	63	VDD	83	DQ16	103	A6	123	DQ25	143	VDD
4	DQ32	24	DQMB4	44	DQ43	64	VDD	84	DQ48	104	A7	124	DQ57	144	VDD
5	DQ1	25	DQMB1	45	VDD	65	\overline{RAS}	85	DQ17	105	A8	125	DQ26		
6	DQ33	26	DQMB5	46	VDD	66	\overline{CAS}	86	DQ49	106	BA0	126	DQ58		
7	DQ2	27	VDD	47	DQ12	67	\overline{WE}	87	DQ18	107	VSS	127	DQ27		
8	DQ34	28	VDD	48	DQ44	68	CKE1	88	DQ50	108	VSS	128	DQ59		
9	DQ3	29	A0	49	DQ13	69	\overline{S}_0	89	DQ19	109	A9	129	VDD		
10	DQ35	30	A3	50	DQ45	70	A12	90	DQ51	110	BA1	130	VDD		
11	VDD	31	A1	51	DQ14	71	\overline{S}_1	91	VSS	111	A10/AP	131	DQ28		
12	VDD	32	A4	52	DQ46	72	A13*	92	VSS	112	A11	132	DQ60		
13	DQ4	33	A2	53	DQ15	73	NC	93	DQ20	113	VDD	133	DQ29		
14	DQ36	34	A5	54	DQ47	74	CLK1	94	DQ52	114	VDD	134	DQ61		
15	DQ5	35	VSS	55	VSS	75	VSS	95	DQ21	115	DQMB2	135	DQ30		
16	DQ37	36	VSS	56	VSS	76	VSS	96	DQ53	116	DQMB6	136	DQ62		
17	DQ6	37	DQ8	57	NC	77	NC	97	DQ22	117	DQMB3	137	DQ31		
18	DQ38	38	DQ40	58	NC	78	NC	98	DQ54	118	DQMB7	138	DQ63		
19	DQ7	39	DQ9	59	NC	79	NC	99	DQ23	119	VSS	139	VSS		
20	DQ39	40	DQ41	60	NC	80	NC	100	DQ55	120	VSS	140	VSS		

(continued on the next page)

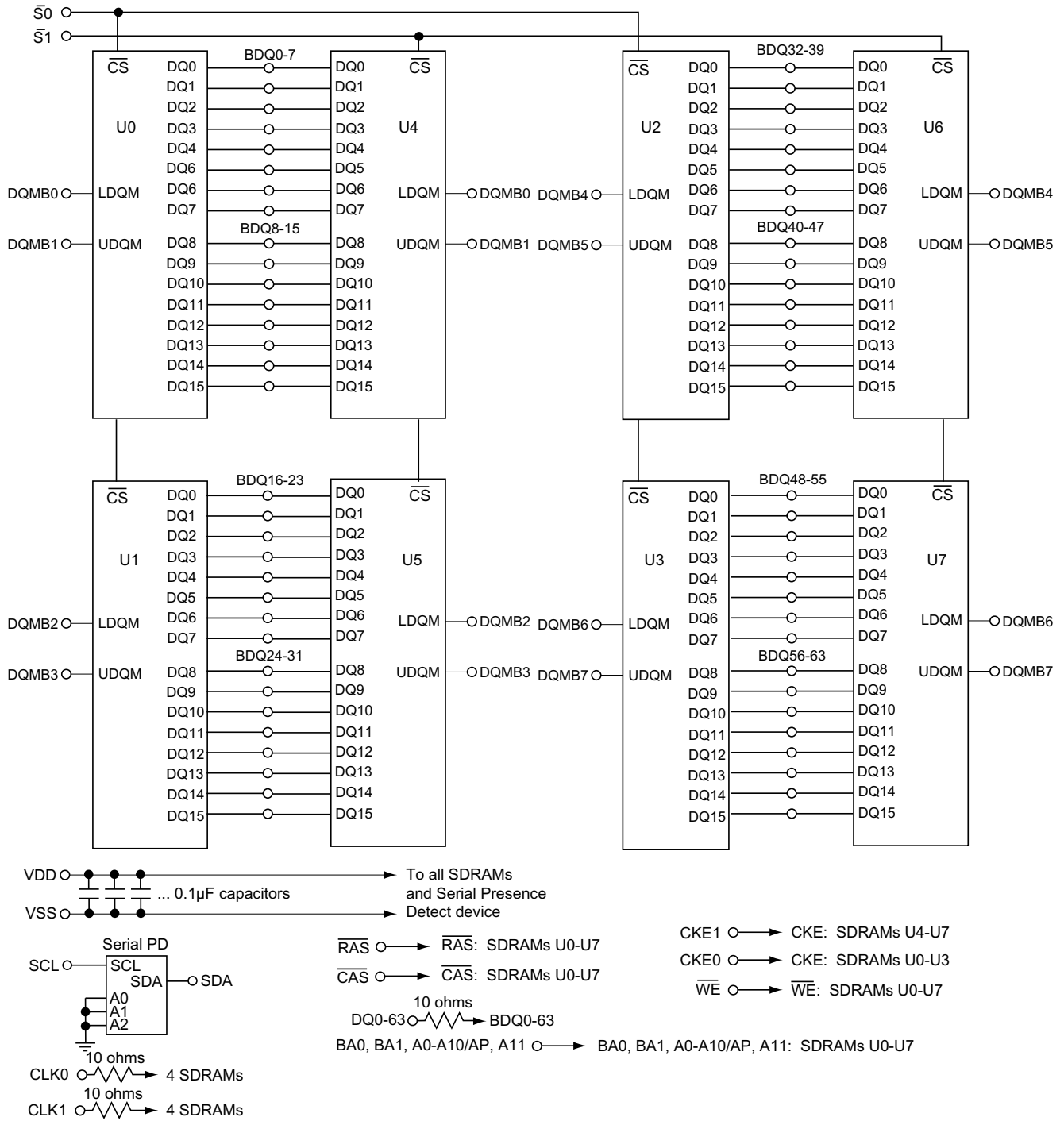
Pin Arrangement



Pin Functions

Pin Name	Pin Function
A0-A10/AP, A11, A12	Address Inputs (multiplexed)
BA0, BA1	Select Bank
DQ0-DQ63	Data In/Out
\overline{WE}	Read/Write Enable
CLK0, CLK1	Clock Input
CKE0, CKE1	Clock Enable Input
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
DQMB0-DQMB7	Data Input/Output Mask
$\overline{S}_0, \overline{S}_1$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I²C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
0	# of bytes written into serial memory at module manufacturer	128 bytes		80h	
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)		08h	
2	Fundamental memory type	SDRAM		04h	
3	# of row addresses on this assembly	13		0Dh	
4	# of column addresses on this assembly	9		09h	
5	# of module ranks on this assembly	2 ranks		02h	
6	Data width of this assembly	64 bits		40h	
7	...Data width of this assembly (continued)	—		00h	
8	Voltage interface standard of this assembly	LVTTL		01h	
9	SDRAM cycle time at CL=3 (t _{CYC})	7.5ns	7.5ns	75h	75h
10	SDRAM access time from clock at CL=3 (t _{AC})	5.4ns	5.4ns	54h	54h
11	DIMM configuration type	none		00h	
12	Refresh rate/type	7.8µs, Self-refresh		82h	
13	SDRAM width	16 bits		10h	
14	Error Checking DRAM data width	none		00h	
15	Min. CLK delay for back-to-back rand. col. addr.	t _{CCD} =1 CLK		01h	
16	SDRAM device attributes: burst lengths supported	1,2,4,8, and full page		8Fh	
17	SDRAM device attributes: # of banks on SDRAM device	4 banks		04h	
18	SDRAM device attributes: CAS latency	CAS latency = 2,3		06h	
19	SDRAM device attributes: CS latency	CS latency = 0		01h	
20	SDRAM device attributes: Write latency	Write Latency = 0		01h	
21	SDRAM module attributes	non-buff., non-reg., non-PLL		00h	
22	SDRAM device attributes: general	V _{CC} 10%, B/R, S/W, P/A, A/P		0Eh	
23	Minimum clock cycle time at CL=2 (t _{CYC})	10ns	7.5ns	A0h	75h
24	Max. data access time form clock at CL=2 (t _{AC})	6ns	5.4ns	60h	54h
25	Minimum clock cycle time at CL=1 (t _{CYC})	—	—	00h	00h
26	Max. data access time from clock at CL=1 (t _{AC})	—	—	00h	00h
27	Minimum row precharge time (t _{RP})	20ns	15ns	14h	0Fh
28	Minimum row active to row active delay (t _{RRD})	15ns	15ns	0Fh	0Fh
29	Minumum RAS to CAS (t _{RCD})	20ns	15ns	14h	0Fh
30	Minumum RAS pulse width (t _{RAS})	45ns	45ns	2Dh	2Dh
31	Module bank density	128MB		20h	
32	Min. command and address signal setup time (t _{AS})	1.5ns		15h	
33	Min. command and address signal hold time (t _{AH})	0.8ns		08h	
34	Min. data signal input setup time (t _{DS})	1.5ns		15h	

(Serial Presence Detect Information continued on the next page)

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte #	Function Described	Function Supported		Hex Value	
		Option A	Option D	Option A	Option D
35	Min. data signal input hold time (t _{DH})	0.8ns		08h	
36-61	Superset information (may be used in future)	—		00h	
62	SPD revision	1.2		12h	
63	Checksum for bytes 0-62	JEDEC calculation		xxh	
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code		7Fh	
65	Man. JEDEC ID code (continued)	STEC's ID		A8h	
66-71				00h	
72	Manufacturing location	STEC USA or STEC Malaysia		01h (USA) or 02h	
73-90	Manufacturer's part number			xxh	
91	Revision code of PCB	RevA(01),RevB(02)		xxh	
92				00h	
93	Manufacturing date	Year (BCD)		yy	
94		Calender Week (BCD)		w w	
95	Assembly serial number	Tester number		ss	
96		Serial number (bits 7-0)		ss	
97		Serial number (bits 15-8)		ss	
98		Serial number (bits 23-16)		ss	
99-125	Manufacturer's specific data			xxh	
126	Intel specification frequency	100MHz		64h	
127	Intel specification details	CLK 0, 1; junc temp TBD CL2, 3; concurrent AP		CFh	

ABSOLUTE MAXIMUM RATINGS¹

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to VSS	V _{IN} , V _{OUT}	-1.0 to +4.6	V
Voltage on VCC Supply Relative to VSS	VDD	-1.0 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	8	W
Short Circuit Output Current	I _{OS}	50	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to VSS=0, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	VDD+0.3	V	1
Input Low Voltage	V _{IL}	-0.3	0	0.8	V	2
Output High Voltage Level	V _{OH}	2.4	—	—	V	I _{OH} = -4mA
Output Low Voltage Level	V _{OL}	—	—	0.4	V	I _{OL} =4mA
Input Leakage Current	I _{IL}	-40	—	40	μA	3
Output Leakage Current	I _{OL}	-10		10		3, 4

- V_{IH}(max)=5.6 V AC (pulse width <=3 ns acceptable).
- V_{IL}(min) = -2.0 V AC (pulse width <=3 ns acceptable).
- Any input 0<=V_{IN}<=VDD.
- Data out is disabled, 0<=V_{OUT}<=VDD.

CAPACITANCE (T_A=23 °C, VDD=3.3V, f=1MHz, VREF=1.4±200mA)

Item	Symbol	Max	Units
Input Capacitance (A, BA, RAS, CAS, WE) 20pF adder for board.	C _{IN1}	50.4	pF
Input Capacitance (CLK) 10pF adder for board.	C _{IN2}	24	pF
Input Capacitance (CKE, S) 20pF adder for board.	C _{IN3}	35.2	pF
Input Capacitance (DQMB) 5pF adder for board.	C _{IN4}	12.6	pF
Input/Output Capacitance (DQ) 5pF adder for board.	C _{IO1}	17	pF

DC CHARACTERISTICS

Recommended operating conditions unless otherwise noted. $T_A=0$ to 70°C .

Parameter/Condition	Symbol	Option D (Max)	Option A (Max)	Units
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t_{RC}^3 t_{RC} (MIN)	IDD1	568	368	mA
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW	IDD2	16	16	mA
STANDBY CURRENT: Active Mode; CKE = HIGH; \overline{CS} = HIGH; All banks active after t_{RCD} met; No accesses in progress	IDD3	320	280	mA
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active	IDD4	688	528	mA
AUTO REFRESH CURRENT: $t_{RFC} = t_{RFC}$ (MIN) CKE = HIGH; \overline{CS} = HIGH	IDD5	808	728	mA
SELF REFRESH CURRENT: Standard CKE \leq 0.2V	IDD7	24	24	mA

Notes:

1. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
2. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
3. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. For Option D, $CL=2$ and $t_{CK}=7.5\text{ns}$. For Option A, $CL=3$ and $t_{CK}=7.5\text{ns}$.
6. For modules with more than one rank, IDD1, IDD4, and IDD5 are specified with one rank in IDD_n and the other ranks in $IDD2$, where n is IDD number in the Symbol column.
7. Values shown for DDR SDRAM components only.
8. Values will differ depending on DRAM parts used on the module.
9. IDD values are calculated using worst case specifications of currently available DRAMs from different manufacturers listed in Ordering Information.

AC TIMING PARAMETERS *(Recommended operating conditions unless otherwise specified.)*

Parameter	Symbol	Option A		Option D		Unit	Notes
		Min	Max	Min	Max		
Clock Period	CL3	tCLK	7.5		7.5		ns
	CL2		10		7.5		ns
Clock High Time (Rated @1.5V)		t _{CH}	2.5		2.5		ns
Clock Low Time		t _{CL}	2.5		2.5		ns
Input Setup Times (Data) (Address/Command & CKE)		t _{SI}	1.5		1.5		ns
			1.5		1.5		
Input Hold Times (Data) (Address/Command & CKE)		t _{HI}	0.8		0.8		ns
			0.8		0.8		
Output Valid From Clock (LVTTL levels; Rated@50pF; all outputswitching)	CL3	t _{AC}		5.4		5.4	ns
	CL2			6		5.4	ns
Output Hold From Clock (Rated@50pF)		t _{OH}	2.7		2.7		ns
CAS to CAS Delay		t _{CCD}	1		1		tCLK
CKE to Clock Disable		t _{CKE}	1		1		tCLK
RAS Precharge Time		t _{RP}	20		15		ns
RAS Active Time		t _{RAS}	45	120K	45	120K	ns
Active to Command Delay (RAS to CAS Delay)		t _{RCD}	20		15		ns
RAS to RAS Bank Activate Delay		t _{RRD}	15		15		ns
RAS Cycle Time		t _{RC}	66		60		ns
DQM to Input Data Delay		t _{DQD}	0		0		tCLK
Write Cmd. to Input Data Delay		t _{DWD}	0		0		tCLK
Mode Register Set to Active Delay		t _{MRD}	2		2		tCLK
Precharge to O/P in High-Z		t _{ROH}		CL		CL	tCLK
DQM to Data in Hi-Z for Read		t _{DQZ}	2		2		tCLK
DQM to Data Mask for Write		t _{DQM}	0		0		tCLK
Data-In to PRE Command Period		t _{DPL}	2		2		tCLK
Data-In to ACT (PRE) Cmd Period (Auto Precharge)		t _{DAL}	4		5		tCLK
Power Down Mode Entry		t _{SB}		1		1	tCLK
Exti Self Refresh to Active Time		t _{XSR}	75		67		ns
Power Down Exit Set Up Time		t _{PDE}	1		1		tCLK
Clock Stop During Self Refresh or Power Down		t _{CLKSTP}	200		200		tCLK
Refresh Period		t _{REF}		64		64	ms

1. Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V. t_{ACN}=access time with 0pF load.
2. CL=CAS Latency.
3. Data Masked on the same clock.
4. Timing is asynchronous. If t_{set} is not met by rising edge of CLK then CKE is assumed latched on next cycle.

5. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
6. 8,192 refresh cycles.

REVISION HISTORY**Rev. Change Description from Previous Revision**

-101 11/14/2007. Initial release.

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