256M x 64 Bit (2GB) 204-Pin DDR3 Small-Outline Unbuffered DIMM (PC3-8500) 2 Ranks x 8; RoHS-6 Compliant

GENERAL DESCRIPTION

The SL64F8W256M8L-A18JTG is a 256M x 64 bit (1GB) 204-pin Double Data Rate 3 (DDR3) Small-Outline Unbuffered Dual In-Line Memory Module (SO-UDIMM).

The module consists of sixteen CMOS 16M x 8 bit x 8 bank DDR3 SDRAMs in lead-free BGA packages mounted in 2 ranks on a 204-pin glass epoxy substrate.

A serial EEPROM using the two pin I^2C protocol is also mounted to provide the Serial Presence Detects (SPD). Decoupling capacitors are mounted across the power supply. Damping resistors are added in series for DQ, DQS and DM signals.

The module has gold edge connections and is intended for mounting into 204-pin UDIMM edge connector sockets keyed for 1.5V.

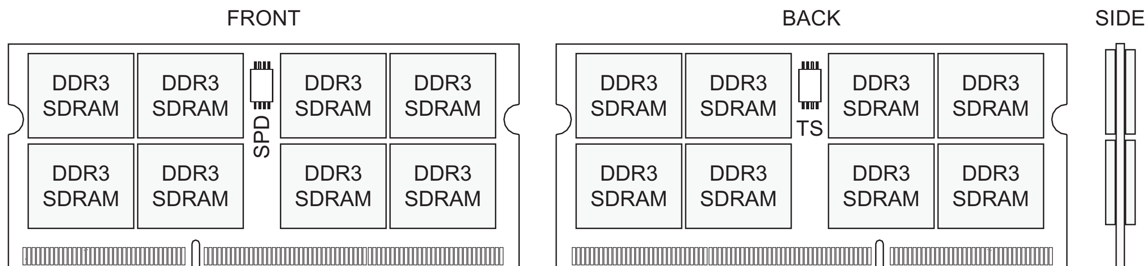
FEATURES

- PC3-8500 Compliant
  (DDR3-1066 533MHz-1.875ns@CL-^{t}RCD-^{t}RP: 7-7-7)
- 204-Pin SO-UDIMM form factor
- Average Periodic Refresh Interval (^{t}REFI)
  - 7.8125ms Max for $0^oC < T_C < 85^oC$
    (64ms/8,196 cycles)
  - 3.9ms Max for $85^oC < T_C < 95^oC$
    (32ms/8,196 cycles)
- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- V_{DDSPD} = 1.425V to 1.575V
- JEDEC Standard 1.5V I/O (SSTL_15 compatible)
- DDR3 Architecture: Two data accesses per clock cycle, differential clock inputs (CK, /CK), bidirectional differential data strobe (DQS, /DQS), Off-Chip Driver (OCD), Impedance Adjustment, Dynamic On-Die Termination (ODT), On-Chip Delay Locked Loop (DLL); Eight-bit prefetch architecture
- Commands entered on each rising CK edge; DQS-edge aligned with data for READs and center-aligned with data for WRITEs; DLL to align DQ and DQS transitions with CK
- Eight internal component banks for concurrent operation
- Asynchronous RESET Pin Support
- ZQ Calibration Support
- Concurrent Auto Precharge option is supported
- Data Mask (DM) for masking Write data
- Programmable Burst Lengths: 4 (Burst Chop) and 8 (Nibble Sequential and Interleave Mode)
- /CAS READ Latency (CL): 6, 7, 8
- /CAS WRITE Latency (CWL): 5, 6 -^{t}CK
- Posted /CAS Additive Latency (AL): 0, CL-1, CL-2
- Adjustable Data-Output drive strength
- Serial Presence Detect (SPD) EEPROM
- Gold edge contacts
- RoHS-6 Compliant and Halogen Free

ORDERING INFORMATION

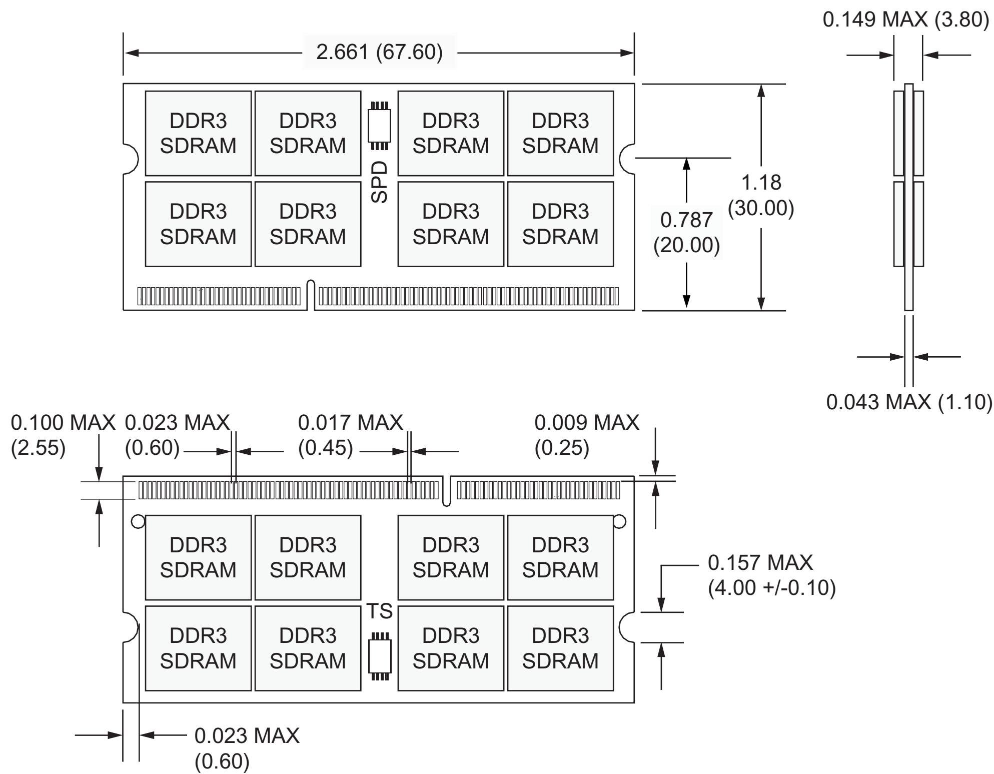
Part Number	Module Speed	Chip Speed	CL-^{t}RCD-^{t}RP
SL64F8W256M8L-A18JTG	PC3-8500	DDR3-1066	7-7-7

204-PIN SO-UDIMM ILLUSTRATION

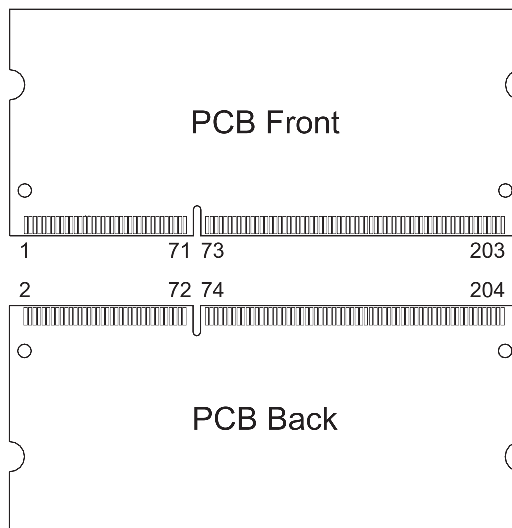


PACKAGE DIMENSIONS *(Board No. 1794)*

Units are in inches (millimeters). All dimensions are typical unless otherwise noted.



PIN LOCATIONS



PIN CONFIGURATION *(* = Not Used; / = Active Low; **Bold Line or Box** = **Key**)*

204-PIN SO-UDIMM PINOUT

204-Pin SO-UDIMM Front								204-Pin SO-UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	53	DQ19	105	VDD	157	DQ42	2	VSS	54	VSS	106	VDD	158	DQ46
3	VSS	55	VSS	107	A10/AP	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	VSS	6	DQ5	58	DQ29	110	/RAS	162	VSS
7	DQ1	59	DQ25	111	VDD	163	DQ48	8	VSS	60	VSS	112	VDD	164	DQ52
9	VSS	61	VSS	113	/WE	165	DQ49	10	/DQS0	62	/DQS3	114	/S0	166	DQ53
11	DM0	63	DM3	115	/CAS	167	VSS	12	DQS0	64	DQS3	116	ODT0	168	VSS
13	VSS	65	VSS	117	VDD	169	/DQS6	14	VSS	66	VSS	118	VDD	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	ODT1	172	VSS
17	DQ3	69	DQ27	121	/S1	173	VSS	18	DQ7	70	DQ31	122	NC	174	DQ54
19	VSS	71	VSS	123	VDD	175	DQ50	20	VSS	72	VSS	124	VDD	176	DQ55
21	DQ8	73	CKE0	125	TEST	177	DQ51	22	DQ12	74	CKE1	126	VREFCA	178	VSS
23	DQ9	75	VDD	127	VSS	179	VSS	24	DQ13	76	VDD	128	VSS	180	DQ60
25	VSS	77	NC	129	DQ32	181	DQ56	26	VSS	78	A15	130	DQ36	182	DQ61
27	/DQS1	79	BA2	131	DQ33	183	DQ57	28	DM1	80	A14	132	DQ37	184	VSS
29	DQS1	81	VDD	133	VSS	185	VSS	30	/RESET	82	VDD	134	VSS	186	/DQS7
31	VSS	83	A12\/BC	135	/DQS4	187	DM7	32	VSS	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	VSS	34	DQ14	86	A7	138	VSS	190	VSS
35	DQ11	87	VDD	139	VSS	191	DQ58	36	DQ15	88	VDD	140	DQ38	192	DQ62
37	VSS	89	A8	141	DQ34	193	DQ59	38	VSS	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	VSS	40	DQ20	92	A4	144	VSS	196	VSS
41	DQ17	93	VDD	145	VSS	197	SA0	42	DQ21	94	VDD	146	DQ44	198	/EVENT
43	VSS	95	A3	147	DQ40	199	VDDSPD	44	VSS	96	A2	148	DQ45	200	SDA
45	/DQS2	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	VSS	202	SCL
47	DQS2	99	VDD	151	VSS	203	VTT	48	VSS	100	VDD	152	/DQS5	204	VTT
49	VSS	101	CK0	153	DM5			50	DQ22	102	CK1*	154	DQS5		
51	DQ18	103	/CK0	155	VSS			52	DQ23	104	/CK1*	156	VSS		

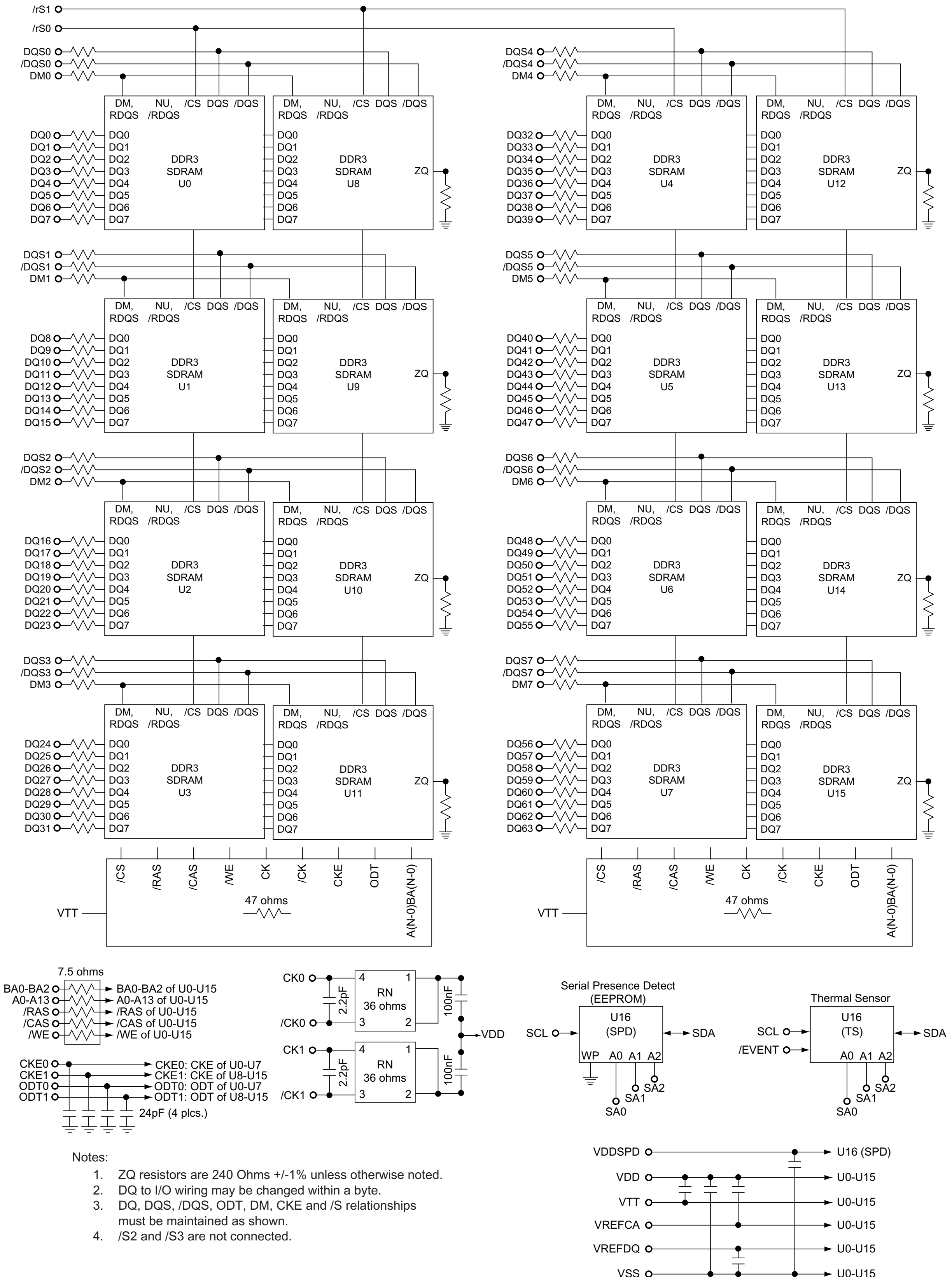
PIN CONFIGURATION *(Continued) (* = Not Used; / = Active Low)*

PIN FUNCTIONS

Symbol	Type	Description
CK0, CK1	Input	Clock Inputs, Positive Line
/CK0, /CK1	Input	Clock Inputs, Negative Line
CKE0, CKE1	Input	Clock Enable
/RAS	Input	Row Address Strobe
/CAS	Input	Column Address Strobe
/WE	Input	Write Enable
/S0, /S1	Input	Chip Select
ODT0, ODT1	Input	On Die Termination
DM0-DM7	Input	Data Masks
DQS0-DQS7	Input/Output	Data Strobes
/DQS0-/DQS7	Input/Output	Data Strobes, Negative
DQ0-DQ63	Input/Output	Data Input/Output
BA0-BA2	Input	Bank Address Inputs
A0-A9, A11, A13-A15	Input	Address Inputs
A10 /AP	Input	Address Input/Autoprecharge
A12 /BC	Input	Address Input/Burst Chop
CB0-CB7*	Input/Output	Data Check Bits
SCL	Input	Serial Clock for Presence Detect
SA0-SA1	Input	Presence Detect Address Inputs
SDA	Input/Output	Serial Presence Detect Data
/RESET	Input	Register and SDRAM Control
NC		No Connect (Reserved for Future Use)
/EVENT		Reserved for Optional Hardware Temperature Testing
TEST		Memory Bus Test Tool (NC and not used for SO-DIMMs)
VDDSPD	Supply	Serial EEPROM/Temp. Sensor Power Supply
VDD	Supply	Core and I/O Power
VSS	Supply	Ground
VREFDQ	Supply	DQ Reference Voltage
VREFCA	Supply	CA Reference Voltage
VTT	Supply	Termination Voltage
PAR_IN*	Input	Parity Bit for the Address and Command Bus ("1": Odd, "0": Even)
ERR_OUT*	Output	Parity Error Found in the Address or Command Bus

FUNCTIONAL BLOCK DIAGRAM

FUNCTIONAL BLOCK DIAGRAM



Notes:

1. ZQ resistors are 240 Ohms +/-1% unless otherwise noted.
2. DQ to I/O wiring may be changed within a byte.
3. DQ, DQS, /DQS, ODT, DM, CKE and /S relationships must be maintained as shown.
4. /S2 and /S3 are not connected.

Functional Block Diagram continued on next page.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol; I^2C; Current sink capability of SDA driver <= 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
0	Number of SPD Bytes Written SPD Device Size CRC Coverage	Size = 256 CRC = 116 Bytes Used = 176	92h
1	SPD Revision	Revision 1.0	10h
2	Key Byte/DRAM Device Type	DDR3 SDRAM	0Bh
3	Key Byte/Module Type	SO-DIMM Width = 67.6mm Nom	03h
4	SDRAM Density and Banks	1Gb Density 8 Internal Banks	02h
5	SDRAM Device Row and Column Count	14 Rows 10 Columns	11h
6	Module Nominal Voltage, V_{DD}	1.5V	00h
7	Module Organization	2 Ranks x8 Device Width	09h
8	Module Memory Bus Width	Non-ECC 64-Bit Primary Bus Width	03h
9	Fine Timebase (FTB) Dividend/Divisor (Pico Seconds)	5/2 = 2.5ps	52h
10	Medium Timebase (MTB) Dividend	1/8 (0.125ns)	01h
11	Medium Timebase (MTB) Divisor	1/8 (0.125ns)	08h
12	SDRAM Minimum Cycle Time, $^{t}CK(min)$	1.875ns	0Fh
13	Reserved	-	00h
14	CAS Latencies Supported Least Significant Byte (LSB)	Low Byte CL Supported = 6, 7, 8	1Ch
15	CAS Latencies Supported Most Significant Byte (MSB)	High Byte CL Supported = 00h	00h
16	CAS Latency Time, $^{t}AA(min)$	13.125ns	69h
17	Write Recovery Time, $^{t}WR(min)$	15ns	78h
18	/RAS to /CAS Delay, $^{t}RCD(min)$	13.125ns	69h
19	Minimum Row Active to Row Active Delay Time, $^{t}RRD(min)$	7.5ns	3Ch
20	Minimum Row Precharge Time, $^{t}RP(min)$	13.125ns	69h
21	^{t}RAS and ^{t}RC Upper Nibbles	- -	11h
22	Min. Active to Precharge Delay Time, $^{t}RAS(min)$, LSB	44ns	2Ch
23	Min. Active to Active Refresh Delay Time, $^{t}RC(min)$, LSB	50.625	95h
24	Min. Refresh Recovery Delay Time, $^{t}RFC(min)$, LSB	110ns	70h
25	Min. Refresh Recovery Time, tRFC(min), MSB	110ns	03h
26	Min. Internal WRITE to READ Command Delay Time, $^{t}WTR(min)$	7.5ns	3Ch

Serial Presence Detect Information continued on next page.

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Serial PD Interface Protocol; I^2C; Current sink capability of SDA driver <= 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
27	Min. Internal READ to PRECHARGE Command Delay Time, $^tRTP(min)$	7.5ns	3Ch
28	Upper Nibble for ^tFAW	-	01h
29	Minimum Four Active Window Delay, $^tFAW(min)$, LSB	37.5ns	2Ch
30	SDRAM Optional Features	DLL-Off Mode not supported RZQ/7 Support	02h
31	SDRAM Thermal and Refresh Options	PASR Extended Temperature Range	81h
32	Module Thermal Sensor	01h = Thermal Sensor	80h
33	Module Thermal Heat Spreader Solution	00h = No Heat Spreader	00h
34	SDRAM Device Type	00h = Standard Monolithic	00h
35 - 59	-	-	00h
60	Module Nominal Height	30 < Height ≤ 31mm	10h
61	Module Maximum Thickness	Back: 1 < Thickness ≤ 2mm Front: 1 < Thickness ≤ 2mm	11h
62	Reference Raw Card Used	Raw Card F, Rev. 0	05h
63	Address Mapping, 1st Rank, Edge Connector to DRAM	Standard	00h
64	RDIMM Thermal Heat Spreader	Heat Spreader	80h
65 - 116	Reserved	-	00h
117 118	Module Manufacturer's JEDEC ID Code	STEC	01h A8h
119	Module ID: Module Manufacturing Location	01h = USA 02h = Malaysia	01h/02h
120 121	Module ID: Module Manufacturing Date		00h 00h
122 123 124 125	Module ID: Module Serial Number		00h 00h 00h 00h
126 127	Cyclical Redundancy Code		01h 01h

Serial Presence Detect Information continued on next page.

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Serial PD Interface Protocol; I^2C; Current sink capability of SDA driver <= 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
128	Module Part Number	S	53h
129		L	4Ch
130		6	36h
131		4	34h
132		F	46h
133		8	38h
134		W	57h
135		2	32h
136		5	35h
137		6	36h
138		M	4Dh
139		8	38h
140		L	4Ch
141		-	2Dh
142		A	41h
143		1	31h
144		8	38h
145		J	4Ah
146	Module Revision Code		00h
147			00h
148	DRAM Manufacturer’s JEDEC ID Code	Qimonda	85h
149			51h
150-175	Manufacturer’s Specific Data		00h
176-255	Open for Customer Use		00h

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages and temperatures for extended periods may affect device reliability.

Symbol	Parameter		Minimum	Maximum	Units
V_{DD}	V_{DD} Supply Voltage relative to V_{SS}		-0.4	1.975	V
V_{DDQ}	V_{DDQ} Supply Voltage relative to V_{SS}		-0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any Pin relative to V_{SS}		-0.4	1.975	V
I_I	Input Leakage Current; Any input 0V <= V_{IN} <= V_{DD}; V_{REF} Input 0V <= V_{IN} <= 0.95V; (All other pins not under test = 0V)	Command/Address	-32	32	µA
		/S, CKE, ODT	-32	32	µA
		CK, /CK	-32	326	µA
		DM	-4	4	µA
I_{OZ}	Output Leakage Current; 0V <= V_{OUT} <= V_{DDQ}; DQS and ODT are disabled	DQ, DQS, /DQS	-10	10	µA
I_{VREF}	V_{REF} Leakage Current; V_{REF} = Valid V_{REF} Level		-18	18	µA
I_{VTT}	Termination Reference Current from V_{TT}		-600	600	mA
V_{TT}	Termination Reference Voltage-Command Address Bus (±20mV)		-0.49 x V_{DD}	+0.51 x V_{DD}	V
T_{STG}	Storage Temperature		-55	100	°C
T_C	Operating Temperature-DRAM Components				
	Commercial Operating Temperature		0	85	°C
	Industrial Operating Temperature: (W) Option		N/A	N/A	°C
T_A	Operating Temperature-Module, Ambient				
	Commercial Operating Temperature		0	70	°C
	Industrial Operating Temperature: (W) Option		N/A	N/A	°C

Notes:

1. Case Temperature, T_C, is the surface temperature on the center/top side of the DRAM. Please refer to the JESD51.2 Standard for the measurement conditions.
2. Case temperature range between 0°C to 85°C is the range which all DRAM specifications are supported.
3. For case temperature ranges between 85°C to 95°C, a doubling of the refresh commands in frequency to a 32ms period (^tREFI = 3.9µs) is required. To enter self-refresh mode at this temperature range, an EMRS command is required to change the internal refresh rate.

RECOMMENDED DC OPERATING CONDITIONS

All voltages referenced to V_{SS}.

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1
V_{DDQ}	I/O Supply Voltage	1.425	1.5	1.575	V	4
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51 x V_{DDQ}	V	2
V_{TT}	I/O Termination Voltage (System)	V_{REF} - 40	V_{REF}	V_{REF} + 40	mV	3

Notes:

1. V_{DD} and V_{DDQ} must track each other. V_{DDQ} must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-Peak noise (non-common mode) on V_{REF} may not exceed $\pm$1 percent of the DC value. Peak-to-Peak AC noise on VREF may not exceed $\pm$2 percent of V_{REF}(DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{DDQ} tracks with V_{DD}; V_{DDL} tracks with V_{DD}.

INPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

INPUT DC LOGIC LEVELS

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IH}(DC)	Input High (Logic 1) Voltage	V_{REF} + 100	TBD	mV	1
V_{IL}(DC)	Input Low (Logic 0) Voltage	-TBD	V_{REF} - 100	mV	1
V_{REFDQ}(DC)	I/O Reference Voltage (DQ)	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	2, 3
V_{REFCA}(DC)	I/O Reference Voltage (CMD/ADD)	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	2, 3
V_{TT}	Termination Voltage	$V_{DDQ}/2$ - TBD	$V_{DDQ}/2$ + TBD	V	2, 3

INPUT AC LOGIC LEVELS

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IH}(AC)	Input High (Logic 1) Voltage	V_{REF} + 175	-	mV	1, 2
V_{IL}(AC)	Input Low (Logic 0) Voltage	-	V_{REF} - 175	mV	1, 2

DIFFERENTIAL INPUT LOGIC LEVELS

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IH}diff	Differential Input High Logic	+200	-	mV	
V_{IL}diff	Differential Input Low Logic	-	-200	mV	
V_{IX}	Differential Cross-Point Voltage relative to $V_{DD}/2$	-150	150	mV	

Notes:

1. For DQ and DM, V_{REF} = V_{REFDQ}. For input only pins except RESET, or V_{REF} = V_{REFCA}.
2. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than $\pm$1% V_{DD} (approximately $\pm$15mV for reference).
3. Approximately $V_{DD}/2$ $\pm$15mV.

OUTPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

AC OUTPUT LEVELS

Symbol	Parameter	Value	Units	Notes
$V_{OH}(AC)$	AC Output High Measurement Level (SR Output)	$V_{TT} + 0.1 \times V_{DDQ}$	V	1
$V_{OL}(AC)$	AC Output Low Measurement Level (SR Output)	$V_{TT} - 0.1 \times V_{DDQ}$	V	1

DC OUTPUT LEVELS

Symbol	Parameter	Value	Units	Notes
$V_{OH}(DC)$	DC Output High Measurement Level (IV Curve Linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OM}(DC)$	DC Output Mid Measurement Level (IV Curve Linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OL}(DC)$	DC Output Low Measurement Level (IV Curve Linearity)	$0.2 \times V_{DDQ}$	V	

DIFFERENTIAL AC and DC OUTPUT PARAMETERS

Symbol	Parameter	Value	Units	Notes
$V_{OH}diff(AC)$	AC Differential Output High Measurement Level (SR Output)	+0.2 x VDDQ	V	2
$V_{OL}diff(DC)$	AC Differential Output Low Measurement Level (SR Output)	-0.2 x VDDQ	V	2

Notes:

1. The swing of $\pm 0.1 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 ohms and an effective test load of 25 ohms to $V_{TT} = V_{DDQ}/2$.
2. The swing of $+0.2 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 ohms and an effective test load of 25 ohms to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs.

IDD SPECIFICATIONS AND CONDITIONS

IDD specifications are tested after the device is properly initialized. Recommended Operating Temperature Range. V_{DD} = +1.5V ±0.075V, V_{DDQ} = +1.5V ±0.075V, V_{DDL} = +1.5V ±0.075V, V_{REF} = V_{DDQ}/2.

Input slew rate is specified by AC Parametric Test Conditions. IDD parameters are specified with ODT disabled. Data bus consists of DQ, DQS, and /DQS. IDD values must be met with all combinations of EMR bits 10 and 11.

Definitions for IDD Conditions:

- LOW is defined as $V_{IN} \le V_{IL}$AC) (MAX).
- HIGH is defined as $V_{IN} \ge V_{IH}$(AC) (MIN).
- STABLE is defined as inputs stable at a HIGH or LOW level.
- FLOATING is defined as inputs at V_{REF} = V_{DDQ}/2.
- SWITCHING is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for *address and control signals*; also defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for *DQ signals* not including masks or strobes.

GENERAL IDD PARAMETERS

IDD Parameter		DDR3-1066	Units
^{t}CKmin(IDD)		1.875	ns
CL(IDD)		7	^{t}CK
^{t}RCDmin(IDD)		13.13	ns
^{t}RCmin(IDD)		50.63	ns
^{t}RASmin(IDD)		37.50	ns
^{t}RPmin(IDD)		13.13	ns
^{t}FAW(IDD)	x4/x8	37.50	ns
	x16	N/A	
^{t}RRD(IDD)	x4/x8	7.5	ns
	x16	N/A	
^{t}RFC(IDD)	512Mb	N/A	ns
	1Gb	110	
	2Gb	N/A	
	4Gb	N/A	

IDD7 CONDITIONS

IDD7: Operating Current, specifies detailed timing requirements for IDD7. Changes will be required if timing parameter changes are made to the specification.

IDD7 OPERATING CURRENT

All Bank Interleave Read operation; legend: **A** = Active; **RA** = Read Auto Precharge; **D** = Deselect
All device banks are being interleaved at minimum ^{t}RC (IDD) without violating ^{t}RRD(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. I_{OUT} = 0mA.

IDD7 Timing Patterns
A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D
A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D

DDR3 IDD SPECIFICATIONS AND CONDITIONS

Symbol	Parameter/Condition
IDD0	Operating One Bank ACTIVATE to PRECHARGE
	CKE = HIGH; External Clock = ON; tCK(MIN); tRC(MIN); tRAS(MIN); /CS = HIGH between ACTIVATE and PRECHARGE; Command Inputs = SWITCHING with exception of ACTIVATE and PRECHARGE commands; Row/Column Addresses = Row Addresses SWITCHING; Address Input A10 = LOW; Bank Address = Fixed; Data I/O = SWITCHING; Output Buffer DQ, DQS = OFF; ODT = DISABLED; Active Banks = Bank 0; ACTIVATE to PRECHARGE Loop.
IDD1	Operating One Bank ACTIVATE to READ to PRECHARGE
	CKE = HIGH; External Clock = ON; tCK(MIN)IDD; tRC(MIN)IDD; tRAS(MIN)IDD; CL IDD; /CS = HIGH between ACTIVATE, READ and PRECHARGE; Command Inputs = SWITCHING with exception of ACTIVATE and PRECHARGE commands; Row/Column Addresses = Row Addresses SWITCHING; Address Input A10 = LOW; Bank Address = Fixed; Data I/O = Read Data: Output data switches after every clock cycle; read data is stable during falling DQS; I/O should be floating when no data read; Output Buffer DQ, DQS = OFF; ODT = DISABLED; Active Banks = Bank 0; ACTIVATE to READ to PRECHARGE Loop.
$IDD2P_{(0)}$	PRECHARGE Power-Down Current (Slow Exit)
	All Device Banks = IDLE; CKE = LOW; External Clock = ON. tCK = tCK(MIN); /CS = STABLE; Command Inputs = STABLE; Row/Column Addresses = STABLE; Bank Addresses = STABLE; Data I/O = FLOATING; Output Buffer DQ, DQS = OFF; ODT = DISABLED; No Active Banks. MR0[12] defines DLL ON/OFF behavior during PRECHARGE power-down only; DLL ON (Fast Exit), MR0[12] = 1) and DLL OFF (Slow Exit, MR0[12] = 0).
$IDD2P_{(1)}$	PRECHARGE Power-Down Current (Fast Exit)
	All Device Banks = IDLE; CKE = LOW; External Clock = ON. tCK = tCK(MIN); /CS = STABLE; Command Inputs = STABLE; Row/Column Addresses = STABLE; Bank Addresses = STABLE; Data I/O = FLOATING; Output Buffer DQ, DQS = OFF; ODT = DISABLED; No Active Banks. ON/OFF behavior during PRECHARGE power-down only; DLL ON (Fast Exit), MR0[12] = 1) and DLL OFF (Slow Exit, MR0[12] = 0).
IDD2Q	PRECHARGE Quiet Standby Current
	All Device Banks = IDLE; CKE = HIGH; External Clock = ON. tCK = tCK(MIN); /CS = STABLE; Command Inputs = STABLE; Row/Column Addresses = STABLE; Bank Addresses = STABLE; Data I/O = FLOATING; Output Buffer DQ, DQS = OFF; ODT = DISABLED.
IDD2N	PRECHARGE Standby Current
	All Device Banks = IDLE; CKE = HIGH; External Clock = ON. tCK = tCK(MIN); /CS = HIGH; Command Inputs = SWITCHING; Row/Column Addresses = SWITCHING; Bank Addresses = SWITCHING; Data I/O = SWITCHING; Output Buffer DQ, DQS = OFF; ODT = DISABLED.
IDD3P	Active Power-Down Current
	All Device Banks = OPEN; CKE = LOW; External Clock = ON; tCK = tCK(MIN); /CS = STABLE; Command Inputs = STABLE; Row/Column Addresses = STABLE; Bank Addresses = STABLE; Data I/O = FLOATING; Output Buffer DQ, DQS = OFF; ODT = DISABLED.
IDD3N	Active Standby Current
	All Device Banks = OPEN; CKE = HIGH; External Clock = ON; tCK = tCK(MIN); /CS is HIGH between valid commands; Command Inputs = SWITCHING; Row/Column Addresses = SWITCHING; Data I/O = SWITCHING; Output Buffer DQ, DQS = OFF; ODT = DISABLED.

DDR3 IDD Specifications and Conditions continued on next page.

DDR3 IDD SPECIFICATIONS AND CONDITIONS *(continued)*

Symbol	Parameter/Condition
IDD4R	Burst READ Operating Current
	All Device Banks = OPEN; CKE = HIGH; External Clock = ON; tCK = tCK(MIN); CL = CL IDD; /CS = HIGH between valid commands; Command Inputs = SWITCHING READ Command Pattern; Column Addresses = SWITCHING; A10 = LOW; Bank Addresses Looping; Data I/O = Read Data Burst (BL8): OUTPUT DATA switches after every clock cycle, read data is STABLE during falling DQS. Output Buffer DQ, DQS = DISABLED; ODT = DISABLED; Burst Length = 8 Fixed (MR0).
IDD4W	Burst WRITE Operating Current
	All Device Banks = OPEN; CKE = HIGH; External Clock = ON; tCK = tCK(MIN); CL = CL IDD; /CS = HIGH between valid commands; Command Inputs = SWITCHING WRITE Command Pattern; Column Addresses = SWITCHING; A10 = LOW; Bank Addresses Looping; Data I/O = Write Data Burst (BL8): INPUT DATA switches after every clock cycle, write data is STABLE during falling DQS. Output Buffer DQ, DQS = DISABLED; ODT = DISABLED; Burst Length = 8 Fixed (MR0)
IDD5B	Burst Refresh Current
	Active Banks = REFRESH command every tRFC(MIN); CKE = HIGH; External Clock = ON; tCK = tCK(MIN); tRC = tRFC(MIN); /CS = HIGH between valid commands; Command Inputs = SWITCHING; Row/Column Addresses = SWITCHING; Bank Addresses = SWITCHING; Data I/O = SWITCHING; Output Buffer DQ, DQS = DISABLED; ODT = DISABLED; .
IDD6	Self Refresh Current – Normal Temperature Range: TC = 0oC - 85°C
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; /CS = FLOATING; Command/Row/Column/Bank/Data I/O = FLOATING; Output Buffer DQ, DQS = DISABLED; ODT = DISABLED; SRT = DISABLED.
$IDD6_{ET}$	Self Refresh Current – Extended Temperature Range: TC = 0oC - 95°C
	CKE = LOW; External Clock = OFF; CK and /CK = LOW; /CS = FLOATING; Command/Row/Column/Bank/Data I/O = FLOATING; Output Buffer DQ, DQS = DISABLED; ODT = DISABLED; SRT = ENABLED.
IDD7	Operating Bank Interleave READ Current
	All Device Banks = INTERLEAVING READS; External Clock = ON; tCK = tCK(MIN); tRC = tRC(MIN); tRAS = tRAS(MIN); tRCD = tRCD(MIN); tRRD = tRRD(MIN); CL = CL IDD; AL = CL-1; /CS = HIGH between valid commands; Row/Column Addresses = STABLE between DESELECTs (DES); Bank Addresses = LOOPING; Data I/O = Read Data (BL8): Output data switches after every clock cycle; read data is STABLE while DQS is falling; I/O = FLOATING when no read data is being driven. Output Buffer DQ, DQS = OFF; ODT = DISABLED; Burst Length = 8 Fixed (MR0).

MAXIMUM DDR3 IDD VALUES

Notes:

1. For IDD0, IDD1, IDD4W, IDD5 and IDD7:

   For a one rank module:

   IDD*n* is calculated with the rank in IDD*n*.

   For two rank modules:

   1. IDD0, IDD1, IDD4W, IDD4R, IDD5 and IDD7 are calculated with one rank in IDD*n* and one rank in IDD2N **and**
   2. IDD2P, IDD2Q, IDD2N, IDD3P, IDD3N and IDD6 are calculated with two ranks in IDD*n*.

   For four rank modules:

   1. IDD0, IDD1, IDD4W, IDD4R, IDD5 and IDD7 are calculated with one rank in IDD*n* and one rank in IDD2N and two ranks in IDD2P, **and**
   2. IDD2P, IDD2Q, IDD2N, IDD3P, IDD3N and IDD6 are calculated with two ranks in IDD*n* and two ranks in IDD2P.

   Where *n* = corresponding IDD condition listed in the Symbol column.

3. Values shown for DDR2 SDRAM components only.
4. Values will differ according to the DRAM parts used to manufacture the module.
5. IDD values are calculated using worst-case specifications of currently available DRAMs from different manufacturers.
6. For Industrial Operating Temperature Range:

   When $T_C \leq 0^oC$:

   1. IDD2P and $IDD3P_{(Slow)}$ must be derated by 4 percent
   2. IDD4R and IDD5W must be derated by 2 percent
   3. IDD6 and IDD7 must be derated by 7 percent

   When $T_C \leq 85^oC$:

   1. IDD0, IDD1, IDD2N, IDD2Q, IDD3N, $IDD3P_{(Fast)}$, IDD4R, IDD4W and IDD5W must be derated by 2 percent
   2. IDD2P must be derated by 20 percent
   3. $IDD3P_{(Slow)}$ must be derated by 30 percent
   4. IDD6 must be derated by 80 percent (IDD6 will increase by this amount if $T_C < 85^oC$ and the 2x refresh option is still enabled)

Symbol	DDR3-1066	Units
IDD0	1,480	mA
IDD1	1,640	mA
$IDD2P_0$	600	mA
$IDD2P_1$	800	mA
IDD2N	840	mA
IDD2Q	1,000	mA
IDD3P	840	mA
IDD3N	1,040	mA
IDD4W	2,320	mA
IDD4R	2,520	mA
IDD5	N/A	mA
$IDD5_B$	2,600	mA
IDD6	576	mA
$IDD6_L$	N/A	mA
$IDD6_{ET}$	592	mA
$IDD6_{TC}$	N/A	mA
IDD7	5,320	mA

CAPACITANCE

V_{DD} = +1.5V ±0.075V, V_{DDQ} = +1.5V ±0.075V, V_{REF} = V_{SS}, *f* = 100 MHz, Recommended Operating Temperature Range, V_{OUT}(DC) = V_{DDQ}/2, V_{OUT}(Peak-to-Peak) = 0.1V. While DM, TDQS, /TDQS have different functions, the loading matches DQ and DQS.

Symbol	Parameter	Maximum	Units
	Input Capacitance:		
C_{CK0}	CK0, /CK0	TBD	pF
C_{CK1}	CK1, /CK1	TBD	pF
C_{CK2}	CK2, /CK2	TBD	pF
	(15pF added for board)		
	Input Capacitance:		
C_{I0}	BA, A, /RAS, /CAS, /WE	TBD	pF
C_{I1}	/S, CKE, ODT	TBD	pF
	(30pF added for board)		
	Input/Output Capacitance:		
$C_{I/O}$	DQ, DQS, /DQS, , TDQS, /TDQS, DM	TBD	pF
	(5pF added for board)		

SPEED BINS - DDR3-1066

Recommended Operating Temperature Range; $V_{DDQ} = V_{DD} = 1.5V \pm 0.075V$

Symbol	Parameter		Minimum	Maximum	Units
^{t}RCD	ACT to Internal READ or WRITE Delay Time		13.125	-	ns
^{t}RP	PRE Command Period		13.125	-	ns
^{t}RC	ACT to ACT or REF Command Period		50.625	-	ns
^{t}RAS	ACT to PRE Command Period		37.50	9 x ^{t}REFI	ns
^{t}CK(avg)	CL = 5	CWL = 5	Reserved		ns
		CWL = 6	Reserved		ns
	CL = 6	CWL = 5	2.5	3.3	ns
		CWL = 6	Reserved		ns
	CL = 7	CWL = 5	Reserved		ns
		CWL = 6	1.875	< 2.5	ns
	CL = 8	CWL = 5	Reserved		ns
		CWL = 6	1.875	< 2.5	ns
	Supported CL Settings		6, 7, 8		nCK
	Supported CWL Settings		5, 6		nCK

SPEED BIN NOTES

1. The CL and CWL settings result in ^{t}CK(AVG).MIN and ^{t}CK(AVG).MAX requirements. When selecting a ^{t}CK(AVG), both need to be fulfilled.
2. ^{t}CK(AVG).MIN limits. CAS Latency is not strictly analog; the data and strobe output are synchronized by the DLL. All possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard ^{t}CK(AVG) value (2.5, 1.875, 1.5 or 1.25 nanoseconds) when calculating CL [*n*CK] = ^{t}AA[ns], rounding up to the next 'supported CL'.
3. ^{t}CK(AVG).MAX limits: ^{t}CK(AVG) = ^{t}AA.MAX/CLSELECTED, rounding the ^{t}CK(AVG) down to the next valid speed bin limit (3.3ns or 2.5ns, or 1.875ns or 1.25ns). This result is ^{t}CK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. The user must program a different value.
5. 'Optional' settings allow certain devices to support this setting, but it is not a mandatory feature. Refer to the datasheet of the supplier and SPD information to determine if and how this setting is supported.
6. Any DDR3 speed bin also supports functional operation at lower frequencies as indicated in the table but are verified by design only and not production tests.
7. ^{t}REFI is dependent on T_C operating temperature (case temperature).

Speed Bins continued on next page.

CLOCK TIMING AND CLOCK JITTER PARAMETERS

Clock Timing	Symbol	Minimum	Maximum	Units
Minimum Clock Cycle Time (DLL Off Mode)	$^{t}CK(DLL_OFF)$	8	7,800	ns
Average Clock Period	$^{t}CK(avg)$	See Speed Bins Table		ps
Average High Pulse Width	$^{t}CH(avg)$	0.47	0.53	
Average Low Pulse Width	$^{t}CH(avg)$	0.47	0.53	
Absolute Clock Period	$^{t}CK(abs)$	tCK(avg) Min + tJIT(per) Min	tCK(avg) Max + tJIT(per) Max	ps
Absolute Clock HIGH Pulse Width	$^{t}CH(abs)$	0.43	-	
Absolute Clock LOW Pulse Width	$^{t}CL(abs)$	0.43	-	
Clock Jitter	**Symbol**	**Minimum**	**Maximum**	**Units**
Clock Period Jitter, DLL Locked	$^{t}JIT(per)$	180		ps
Clock Period Jitter during DLL Locking Period	$^{t}JIT(per_tck)$	160		ps
Cycle to Cycle Period Jitter	$^{t}JIT(cc)$	-	-	ps
Cycle to Cycle Period Jitter during DLL Locking Period	$^{t}JIT(cc_tck)$	-	-	ps
Duty Cycle Jitter	$^{t}JIT(duty)$	-	-	
Cumulative Jitter Error, 2 Cycles	$^{t}ERR(2per)$	-132	132	ps
Cumulative Jitter Error, 3 Cycles	$^{t}ERR(3per)$	-157	157	ps
Cumulative Jitter Error, 4 Cycles	$^{t}ERR(4per)$	-175	175	ps
Cumulative Jitter Error, 5 Cycles	$^{t}ERR(5per)$	-188	188	ps
Cumulative Jitter Error, 6 Cycles	$^{t}ERR(6per)$	-200	200	ps
Cumulative Jitter Error, 7 Cycles	$^{t}ERR(7per)$	-209	209	ps
Cumulative Jitter Error, 8 Cycles	$^{t}ERR(8per)$	-217	217	ps
Cumulative Jitter Error, 9 Cycles	$^{t}ERR(9per)$	-224	224	ps
Cumulative Jitter Error, 10 Cycles	$^{t}ERR(10per)$	-231	231	ps
Cumulative Jitter Error, 11 Cycles	$^{t}ERR(11per)$	-237	237	ps
Cumulative Jitter Error, 12 Cycles	$^{t}ERR(12per)$	-242	242	ps
Cumulative Jitter Error, *n = 13, 14, …49, 50 Cycles* Note: $^{t}ERR(n\text{per})min = (1 + 0.68\ln(n)) * {}^{t}JIT(per)min$ Note: $^{t}ERR(n\text{per})max = (1 + 0.68\ln(n)) * {}^{t}JIT(per)max$	$^{t}ERR(n\text{per})$	See Notes		ps

Clock and Clock Jitter Parameters continued on next page.

CLOCK JITTER NOTES

1. The unit, '^{t}CK(avg)', represents the actual ^{t}CK(avg) of the input clock under operation; 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
2. These parameters are measured from a command/address signal (CKE, /CS, /RAS, /CAS, /WE ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal crossing. The specific values are not affected by the amount of clock jitter applied. The setup and hold are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present or absent.
3. These parameters are measured from a data strobe signal crossing to its respective clock signal crossing. The specific values are not affected by the amount of clock jitter applied. The setup and hold are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present or absent.
4. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc) transition edge to its respective data strobe signal (DQS(L/U)/DQS(L/U) crossing.
5. The DDR3 SDRAM device supports ^{t}nPARM [nCK] = RU{^{t}PARM [ns] / ^{t}CK(avg)}, which is in clock cycles, with the assumption that all input clock jitter specifications are satisfied.
6. The parameters are specified per their average values; however, the relationship between the average timing and the absolute instantaneous timing holds at all times.

TIMING PARAMETERS *(continued)*

Data Timing	Symbol	Minimum	Maximum	Units
DQS, /DQS to DQ Skew, per Group, per Access	^{t}DQSQ	-	150	ps
DQ Output Hold Time from DQS, /DQS	^{t}QH	0.38	-	^{t}CK(avg)
DQ Low-Impedance Time from CK, /CK	^{t}LZ(DQ)	-600	300	ps
DQ High-Impedance Time from CK, /CK	^{t}HZ(DQ)	-	300	ps
Data Setup Time to DQS, /DQS referenced to VIH(AC) VIL(AC) Levels	^{t}DS(base)	-	-	ps
Data Hold Time to DQS, /DQS referenced to VIH(AC) VIL(AC) Levels	^{t}DH(base)	-	-	ps
Data Strobe Timing	**Symbol**	**Minimum**	**Maximum**	**Units**
DQS, /DQS READ Preamble	^{t}RPRE	0.9	-	^{t}CK
DQS, /DQS Differential READ Postamble	^{t}RPST	0.3	-	^{t}CK
DQS, /DQS Output High Time	^{t}QSH	0.38	-	^{t}CK(avg)
DQS, /DQS Output Low Time	^{t}QSL	0.38	-	^{t}CK(avg)
DQS, /DQS WRITE Preamble	^{t}WPRE	0.9	-	^{t}CK
DQS, /DQS WRITE Postamble	^{t}WPST	0.3	-	^{t}CK
DQS, /DQS Rising Edge Output Access Time from Rising CK, /CK	^{t}DQSCK	-300	300	ps
DQS, /DQS Low-Impedance Time (Referenced from RL-1)	^{t}LZ(DQS)	-600	300	ps
DQS, /DQS High-Impedance Time (Referenced from RL+BL/2)	^{t}HZ(DQS)	-	300	ps
DQS, /DQS Differential Input Low Pulse Width	^{t}DQSL	0.45	0.55	^{t}CK(avg)
DQS, /DQS Differential Input High Pulse Width	^{t}DQSH	0.45	0.55	^{t}CK(avg)
DQS, /DQS Rising Edge to CK, /CK Rising Edge	^{t}DQSS	-0.25	0.25	^{t}CK(avg)
DQS, /DQS Falling Edge Setup Time to CK, /CK Rising Edge	^{t}DSS	0.2	-	^{t}CK(avg)
DQS, /DQS FAlling Edge Hold Time to CK, /CK Rising Edge	^{t}DSH	0.2	-	^{t}CK(avg)

Timing Parameters continued on next page.

TIMING PARAMETERS *(continued)*

Command and Address Timing	Symbol	Minimum	Maximum	Units
DLL Locking Time	^{t}DLLK	512	-	*n*CK
Internal READ Command to PRECHARGE Command Delay	^{t}RTP	Max (4nCK, 7.5ns)	-	
Delay from Start of Internal WRITE Transaction to Internal READ Command	^{t}WTR	Max (4nCK, 7.5ns)	-	
WRITE Recovery Time	^{t}WR	15	-	ns
Mode Register Set Command Cycle Time	^{t}MRD	4	-	^{t}CK(avg)
Mode Register Set Command Update Delay	^{t}MOD	Max (12nCK, 15ns)	-	
ACT to Internal READ or WRITE Delay Time	^{t}RCD	See Speed Bins Table		
PRE Command Period	^{t}RP	See Speed Bins Table		
ACT to ACT or REF Command Period	^{t}RC	See Speed Bins Table		
/CAS to /CAS Command Delay	^{t}CCD	4	-	
Auto Precharge Write Recovery + Precharge Time	^{t}DAL(min)	WR + roundup(^{t}RP/^{t}CK(avg))		*n*CK
Multi-Purpose Register Recovery Time	^{t}MPRR	1	-	
ACTIVE to PRECHARGE Command Period	^{t}RAS	See Speed Bins Table		
ACTIVE to ACTIVE Command Period, 1KB Page Size	^{t}RRD	Max (4nCK, 6ns)	-	
ACTIVE to ACTIVE Command Period, 2KB Page Size	^{t}RRD	Max (4nCK, 7.5ns)	-	
Four Activate Window, 1KB Page Size	^{t}FAW	37.5	-	ns
Four Activate Window, 2KB Page Size	^{t}FAW	50	-	ns
Command and Address Setup Time to CK, /CK referenced to VIH(AC)/VIL(AC) Levels	^{t}IS(base)	TBD	-	ps
Command and Address Hold Time to CK, /CK referenced to VIH(AC)/VIL(AC) Levels	^{t}IH(base)	TBD	-	ps
Calibration Timing	**Symbol**	**Minimum**	**Maximum**	**Units**
Power-Up and RESET Calibration Time	^{t}ZQinitl	512	-	^{t}CK
Normal Operation Full Calibration Time	^{t}ZQoper	256	-	^{t}CK
Normal Operation Short Calibration Time	^{t}ZQCS	64	-	^{t}CK
Reset Timing	**Symbol**	**Minimum**	**Maximum**	**Units**
Exit Reset from CKE HIGH to a Valid Command	^{t}XPR	Max(5nCK, tRFC + 10ns)	-	

Timing Parameters continued on next page.

TIMING PARAMETERS *(continued)*

Power Down Timings	Symbol	Minimum	Maximum	Units
Exit Power Down with DLL ON to any Valid Command; Exit Precharge Power Down with DLL frozen to Commands that ***do not require*** a locked DLL	^{t}XP	Max (3nCK, 7.5ns)	-	
Exit Precharge Power Down with DLL frozen to Commands that ***do require*** a locked DLL	^{t}XPDLL	Max (10^{t}CK, 24ns)	-	
CKE Minimum Pulse Width	^{t}CKE	Max 3(^{t}CK, 5ns)	-	
Command Pass Disable Delay	^{t}CPDED	1	-	nCK
Power Down Entry to Exit Timing	^{t}PD	^{t}CKE(min)	9 x ^{t}REFI	^{t}CK
Timing of ACT Command to Power Down Entry	^{t}ACTPDEN	1	-	nCK
Timing of PRE or PREA Command to Power Down Entry	^{t}PRPDEN	1	-	nCK
Timing of RD/RDA Command to Power Down Entry	^{t}RDPDEN	RL + 4 + 1	-	
Timing of WR Command to Power Down Entry (BL8OTF, BL8MRS, BL4OTF)	^{t}WRPDEN	WL + 4 + (^{t}WR/^{t}CK)	-	nCK
Timing of WRA Command to Power Down Entry (BL8OTF, BL8MRS, BL4OTF)	^{t}WRAPDEN	WL + 4 + WR + 1	-	nCK
Timing of WR Command to Power Down Entry (BL4MRS)	^{t}WRPDEN	WL + 2 + (^{t}WR/^{t}CK)	-	nCK
Timing of WRA Command to Power Down Entry (BL4MRS)	^{t}WRAPDEN	WL + 2 + WR + 1	-	nCK
Timing of REF Command to Power Down Entry	^{t}REFPDEN	1	-	
Timing of MRS Command to Power Down Entry	^{t}MRSDEN	^{t}MOD(min)	-	^{t}CK
ODT Timings	**Symbol**	**Minimum**	**Maximum**	**Units**
ODT High Time without WRITE Command or with WRITE Command and BC4	ODTH4	4	-	nCK
ODT High Time with WRITE Command and BL8	ODTH8	6	-	nCK
Asynchronous RTT Turn-On Delay (Power-Down with DLL Frozen)	^{t}AONPD	1	9	ns
Asynchronous RTT Turn-Off Delay (Power-Down with DLL Frozen)	^{t}AOFPD	1	9	ns
RTT Turn-On	^{t}AON	-225	225	ps
RTT_NOM and RTT_WR Turn-Off Time from ODTLoff Reference	^{t}AOF	0.3	0.7	^{t}CK(avg)
RTT Dynamic Change Skew	^{t}ADC	0.3	0.7	^{t}CK(avg)

Timing Parameters continued on next page.

TIMING PARAMETERS *(continued)*

Self-Refresh Timings	Symbol	Minimum	Maximum	Units
Exit Self-Refresh to Commands that ***do not require*** a Locked DLL	^{t}XS	Max (5nCK, ^{t}RFC + 10ns)	-	
Exit Self-Refresh to Commands that ***do require*** a Locked DLL	$^{t}XSDLL$	$^{t}DLLK(min)$	-	^{t}CK
Minimum CKE Low Width for Self-Refresh Entry to Exit Timing	$^{t}CKESR$	$^{t}CKE(min)$ +1^{t}CK	-	
Valid Clock Requirement after Self-Refresh Entry (SRE) after Self-Refresh Entry (SRE) or Power-Down Entry (PDX)	$^{t}CKSRE$	Max (5^{t}CK, 10ns)	-	
Valid Clock Requirement before Self-Refresh Entry, SRE before Self-Refresh Entry (SRE), Power-Down Exit (PDE)	$^{t}CKSRX$	Max (5^{t}CK, 10ns)	-	
or Reset Exit				

TIMING PARAMETER NOTES

1. Actual values are dependent on measurement level definitions. TBD.
2. READ (and RAP) and synchronous ODT commands require a locked DLL.
3. The maximum values are dependent on the system.
4. WR as programmed in the mode register.
5. RTT Turn-On Time (tAON) TBD.
6. RTT Turn-Off Time (tAOF) TBD.
7. ^{t}WR is in nanoseconds. To calculate $^{t}WRPDEN$, $^{t}WR/^{t}CK$ must be rounded up to the next integer.
8. WR is in clock cycles as programmed in MR0.
9. The maximum postamble is bound by $^{t}HZDQS(max)$.
10. Output timing deratings are relative to the SDRAM input clock. When the device operates with input clock jitter, the parameters need to be derated by TBD.
11. The TBD value is only valid for RON34.
12. TBD is a single-ended signal parameter.
13. $^{t}REFI$ is dependent on T_C.
14. $^{t}IS(base)$ and $^{t}IH(base)$ values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, /CK differential slew rate. For DQ and DM signals, $V_{REF}(DC) = V_{Ref}DQ(DC)$. For input pins except RESET, $V_{Ref}(DC) = V_{Ref}CA(DC)$.
15. $^{t}DS(base)$ and $^{t}DH(base)$ values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, /DQS differential slew rate. For DQ and DM signals, $V_{REF}(DC) = V_{Ref}DQ(DC)$. For input pins except RESET, $V_{Ref}(DC) = V_{Ref}CA(DC)$.
16. The start of the internal write transaction is as follows:
    - For BL8 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
    - For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
    - For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
17. CKE is allowed to register LOW while operations such as row activation, precharge, autoprecharge, autoprecharge or refresh rate are in progress; however, the power-down IDD specification is not applied until such operations are completed.
18. CKE is allowed to register LOW after a REFRESH command once $^{t}REFPDEN(min)$ is satisfied; however, there are situations where additional time such as $^{t}XPDLL(min)$ is also required.
19. $^{t}JIT(duty)$ = +/-{0.07 * $^{t}CK(avg)$ - [p.5 - (min ($^{t}CH(avg)$, $^{t}CL(avg)$)) * $^{t}CK(avg)$]}. For example, if $^{t}CH/tCL$ was 0.48/0.52, ^{t}JIT duty would calculate out to +/- 125ps. The values listed for $^{t}CH(avg)$ and $^{t}CL(avg)$ must not be exceeded.

REVISION HISTORY

Revision	Date	Description
-101	09/24/2008	Initial release.

DISCLAIMER OF LIABILITY

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