

64M x 64 Bit (512MB) 184-Pin Unbuffered DDR DIMM (PC2700), 1 Rank x 8; RoHS-6 Compliant

FEATURES

- PC2700 Compliant
(DDR333 166MHz-6ns@CL-^tRCD-^tRP: 2.5-3-3 Clks)
- 184-Pin UDIMM form factor
- Industrial Operating Temperature Rating:
 - T_A = -40°C to +85°C (Ambient)
 - T_C = -40°C to +95°C (Case)
- Auto and Self-Refresh Capability
(8,192 cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- +2.5V ± 0.2 V_{DD} and V_{DDQ}
- DDR Architecture: Two data accesses per clock cycle, differential clock inputs (CK0, /CK0) and bidirectional differential data strobe (DQS)
- Four internal component banks for concurrent operation
- Auto Precharge option for each burst access
- Burst Lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect (SPD) EEPROM
- Gold edge contacts
- RoHS-6 Compliant

GENERAL DESCRIPTION

The SL64C8M64M8L-A06EWWU is a 64M x 64 bit (512MB) 184-pin Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Unbuffered Dual In-Line Memory Module (UDIMM).

The module consists of eight CMOS 16M x 8 bit x 4 bank DDR SDRAMs in lead-free 66-pin 400-mil TSOP-II packages mounted in 1 rank on a 184-pin glass epoxy substrate. The SDRAMs are rated for industrial temperature operating conditions.

A serial EEPROM using the two pin I²C protocol is also mounted to provide the Serial Presence Detects (SPD). Decoupling capacitors are mounted in parallel across the power supply. Damping resistors are added in series for DQ, DQS and DM signals.

The module has gold edge connections and is intended for mounting into 184-pin UDIMM edge connector sockets keyed for 2.5V V_{DD} and V_{DDQ} .

ORDERING INFORMATION

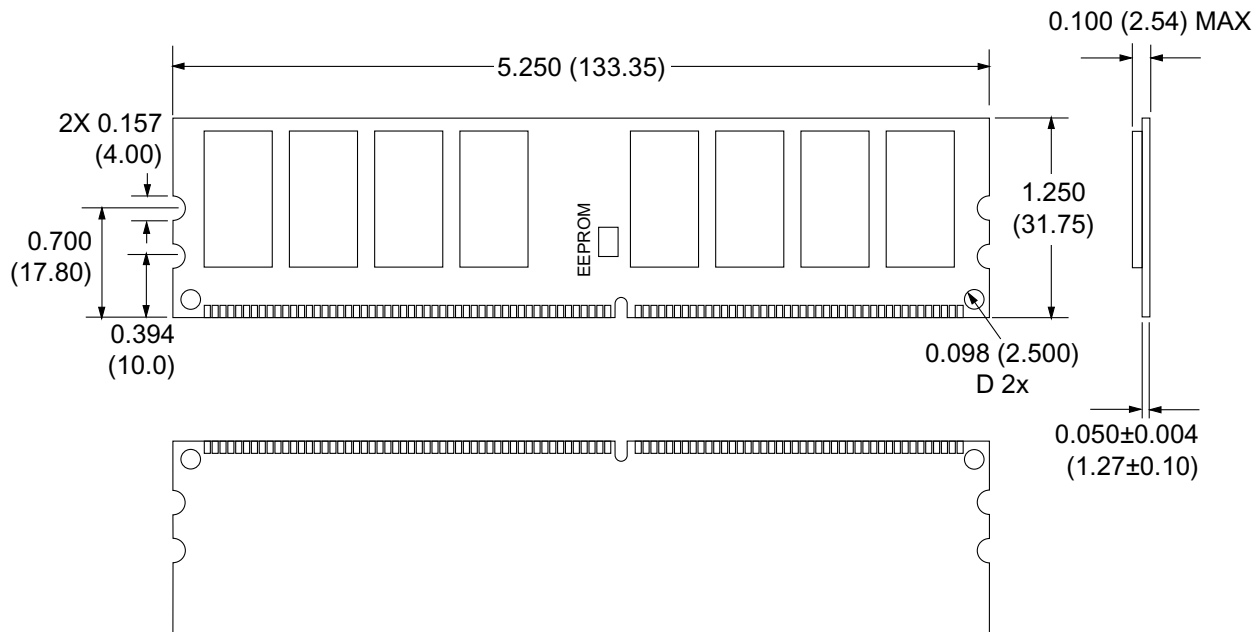
| Part Number | CL | MHz | Bandwidth |
|----------------------|-----|-----|-----------|
| SL64C8M64M8L-A06EWWU | 2.5 | 166 | 2.7 GB/s |

DRAM MANUFACTURERS LIST

| Manufacturer | Part Number | Die Rev |
|--------------|--------------------|---------|
| Micron | MT46V64M8P-6T IT:F | F-Die |

PACKAGE DIMENSIONS (Board No. 855)

Units are in inches (millimeters). Tolerances are +0.005 (+0.127) unless otherwise specified.



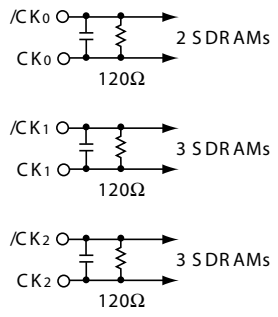
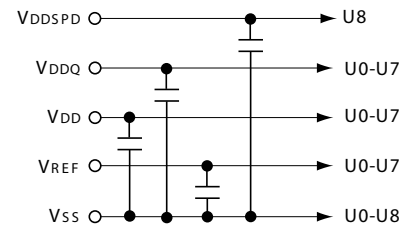
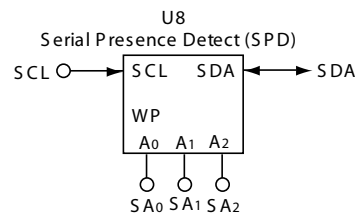
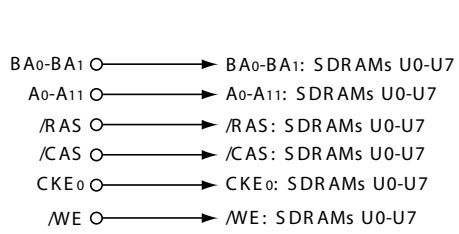
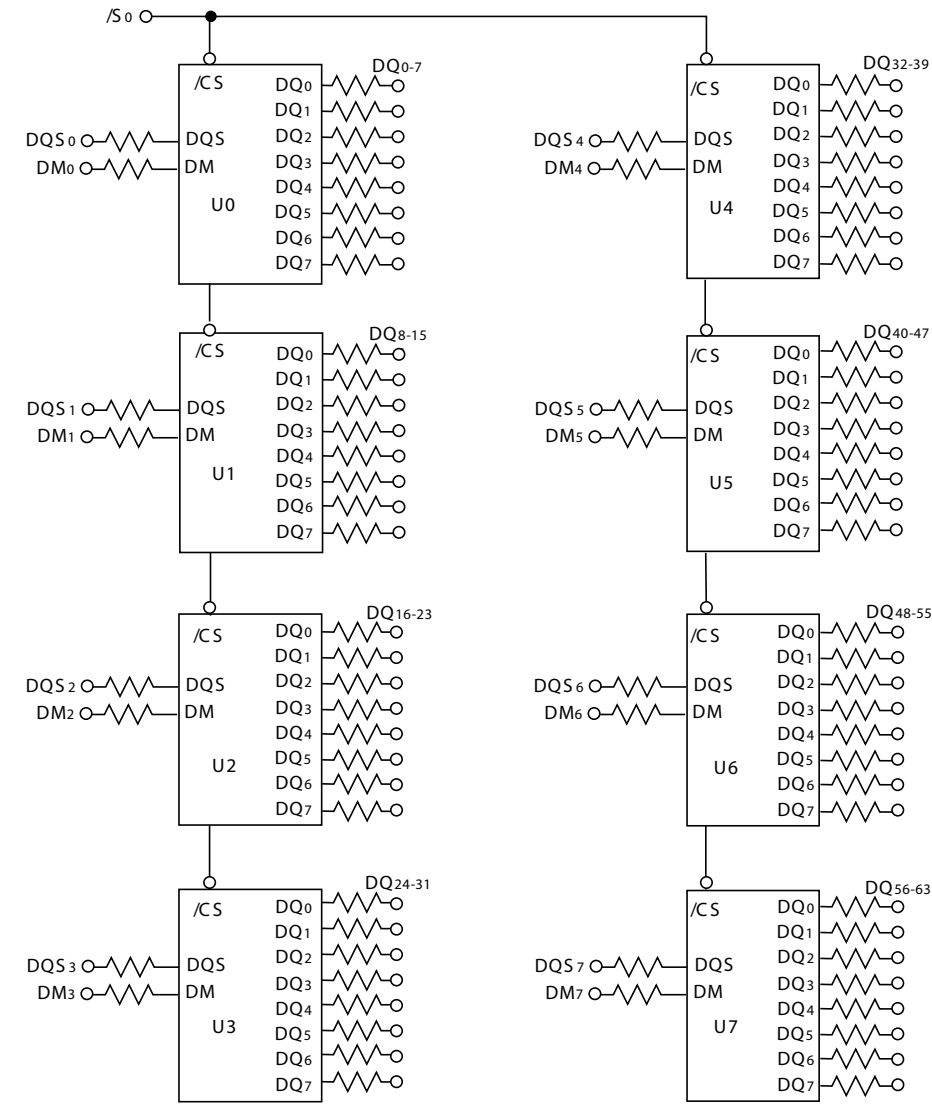
PIN CONFIGURATION (* = Not Used; / = Active Low; **Bold Line or Box** = Key)**184-PIN UDIMM PINOUT**

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|---------|-----|--------|-----|-------|-----|------|-----|-------|-----|--------|
| 1 | VREF | 93 | VSS | 32 | A5 | 124 | VSS | 62 | VDDQ | 154 | /RAS |
| 2 | DQ0 | 94 | DQ4 | 33 | DQ24 | 125 | A6 | 63 | /WE | 155 | DQ45 |
| 3 | VSS | 95 | DQ5 | 34 | VSS | 126 | DQ28 | 64 | DQ41 | 156 | VDDQ |
| 4 | DQ1 | 96 | VDDQ | 35 | DQ25 | 127 | DQ29 | 65 | /CAS | 157 | /S0 |
| 5 | DQS0 | 97 | DM0 | 36 | DQS3 | 128 | VDDQ | 66 | VSS | 158 | /S1* |
| 6 | DQ2 | 98 | DQ6 | 37 | A4 | 129 | DM3 | 67 | DQS5 | 159 | DM5 |
| 7 | VDD | 99 | DQ7 | 38 | VDD | 130 | A3 | 68 | DQ42 | 160 | VSS |
| 8 | DQ3 | 100 | VSS | 39 | DQ26 | 131 | DQ30 | 69 | DQ43 | 161 | DQ46 |
| 9 | NC | 101 | NC | 40 | DQ27 | 132 | VSS | 70 | VDD | 162 | DQ47 |
| 10 | /RESET* | 102 | NC | 41 | A2 | 133 | DQ31 | 71 | /S2* | 163 | /S3* |
| 11 | VSS | 103 | FETEN* | 42 | VSS | 134 | CB4* | 72 | DQ48 | 164 | VDDQ |
| 12 | DQ8 | 104 | VDDQ | 43 | A1 | 135 | CB5* | 73 | DQ49 | 165 | DQ52 |
| 13 | DQ9 | 105 | DQ12 | 44 | CB0* | 136 | VDDQ | 74 | VSS | 166 | DQS3 |
| 14 | DQS1 | 106 | DQ13 | 45 | CB1* | 137 | CK0 | 75 | CK2 | 167 | A13* |
| 15 | VDDQ | 107 | DM1 | 46 | VDD | 138 | /CK0 | 76 | /CK2 | 168 | VDD |
| 16 | CK1 | 108 | VDD | 47 | DQS8* | 139 | VSS | 77 | VDDQ | 169 | DM6 |
| 17 | /CK1 | 109 | DQ14 | 48 | A0 | 140 | DM8* | 78 | DQS6 | 170 | DQ54 |
| 18 | VSS | 110 | DQ15 | 49 | CB2* | 141 | A10 | 79 | DQ50 | 171 | DQ55 |
| 19 | DQ10 | 111 | CKE1* | 50 | VSS | 142 | CB6* | 80 | DQ51 | 172 | VDDQ |
| 20 | DQ11 | 112 | VDDQ | 51 | CB3* | 143 | VDDQ | 81 | VSS | 173 | NC |
| 21 | CKE0 | 113 | BA2* | 52 | BA1 | 144 | CB7* | 82 | VDDID | 174 | DQ60 |
| 22 | VDDQ | 114 | DQ20 | Key | | Key | | 83 | DQ56 | 175 | DQ61 |
| 23 | DQ16 | 115 | A12 | 53 | DQ32 | 145 | VSS | 84 | DQ57 | 176 | VSS |
| 24 | DQ17 | 116 | VSS | 54 | VDDQ | 146 | DQ36 | 85 | VDD | 177 | DM7 |
| 25 | DQS2 | 117 | DQ21 | 55 | DQ33 | 147 | DQ37 | 86 | DQS7 | 178 | DQ62 |
| 26 | VSS | 118 | A11 | 56 | DQS4 | 148 | VDD | 87 | DQ58 | 179 | DQ63 |
| 27 | A9 | 119 | DM2 | 57 | DQ34 | 149 | DM4 | 88 | DQ59 | 180 | VDDQ |
| 28 | DQ18 | 120 | VDD | 58 | VSS | 150 | DQ38 | 89 | VSS | 181 | SA0 |
| 29 | A7 | 121 | DQ22 | 59 | BA0 | 151 | DQ39 | 90 | NC | 182 | SA1 |
| 30 | VDDQ | 122 | A8 | 60 | DQ35 | 152 | VSS | 91 | SDA | 183 | SA2 |
| 31 | DQ19 | 123 | DQ23 | 61 | DQ40 | 153 | DQ44 | 92 | SCL | 184 | VDDSPD |

PIN CONFIGURATION (Continued) (* = Not Used; / = Active Low)**PIN FUNCTIONS**

| Symbol | Description |
|-----------------------|--|
| A0-A11, A12, A13* | SDRAM Address Bus |
| BA0-BA1, BA2* | SDRAM Bank Select |
| DQ0-DQ63 | DIMM Memory Data Bus |
| CB0*-CB7* | DIMM ECC Check Bits |
| /RAS | SDRAM Row Address Strobe |
| /CAS | SDRAM Column Address Strobe |
| /WE | SDRAM Write Strobe |
| /S0, /S1*, /S2*, /S3* | SDRAM Chip Select Lines (Physical Ranks 0, 1, 2 and 3) |
| CKE0, CKE1* | SDRAM Clock Enable Lines |
| DQS0-DQS7, DQS8* | SDRAM Data Strobes |
| DM0-DM7, DM8* | SDRAM Data Mask |
| CK0, CK1, CK2 | SDRAM Clock (Positive Line of Differential Pair) |
| /CK0, /CK1, /CK2 | SDRAM Clock (Negative Line of Differential Pair) |
| SCL | IIC Serial Bus Clock for EEPROM |
| SDA | IIC Serial Bus Data Line for EEPROM |
| SA0-SA2 | IIC Slave Address Select for EEPROM |
| VDD | SDRAM Positive Power Supply |
| VDDQ | SDRAM I/O Driver Positive Power Supply |
| VDDID | VDD Identification Flag (No Connect for VDD = VDDQ) |
| VREF | SDRAM I/O Reference Supply |
| VSS | Power Supply Return (Ground) |
| VDDSPD | Serial EEPROM Positive Power Supply (2.2V to 5.5V) |
| NC | Spare Pins (No Connect) |
| /RESET* | Reset Pin (Forces Register Inputs Low) |
| FETEN* | FET Enable Line |

FUNCTIONAL BLOCK DIAGRAM



- NOTES:
1. DQ wiring may be changed within a byte.
 2. DQ, DQS, DM, CKE, /S relationships must be maintained as shown.
 3. DQ, DQS, and DM resistors are 22Ω.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol; I²C; Current sink capability of SDA driver <= 3mA; Maximum Clock Frequency: 100KHz

| Byte | Description | Entry | Hex Value |
|------|--|--|-----------|
| 0 | Number of SPD Bytes used by Manufacturer | 128 | 80h |
| 1 | Total Number of Bytes in SPD Device | 256 | 08h |
| 2 | Fundamental Memory Type | DDR SDRAM | 07h |
| 3 | Number of Row Addresses on Assembly | 13 | 0Dh |
| 4 | Number of Column Addresses on Assembly | 11 | 0Ah |
| 5 | Number of Physical Banks on Assembly | 1 | 01h |
| 6 | Data Width of the Assembly | 64 | 40h |
| 7 | ...Data Width of the Assembly (continued) | - | 00h |
| 8 | Module Voltage Interface Level | SSTL 2.5V | 04h |
| 9 | SDRAM Cycle Time at CL = 2.5 (t _{CYC}) | 6ns | 60h |
| 10 | SDRAM Access from Clock at CL = 2.5 (t _{AC}) | 0.7ns | 70h |
| 11 | DIMM Configuration Type | No Address or Command Parity Non-ECC Data | 00h |
| 12 | Refresh Rate/Type | 7.8μs/Self-Refresh | 82h |
| 13 | SDRAM Width | x8 | 08h |
| 14 | Error-Checking SDRAM Data Width | None | 00h |
| 15 | Min. CLK Delay for Back-to-Back Rand. Col. Addr. | t _{CCD} = 1 CLK | 01h |
| 16 | Burst Lengths Supported | 2, 4, 8 | 0Eh |
| 17 | Number of Banks on SDRAM Device | 4 | 04h |
| 18 | CAS Latencies Supported | 2.0, 2.5 | 0Ch |
| 19 | CS Latencies Supported | CAS Latency = 0 | 01h |
| 20 | Write Latencies Supported | Write Latency = 1 | 02h |
| 21 | SDRAM Module Attributes | No Register, No PLL Differential Clock | 20h |
| 22 | SDRAM Device Attributes: General | VDD±0.2V | 00h |
| 23 | Min. CLK Cycle Time at CL = 2 (t _{CYC}) | 7.5ns | 75h |
| 24 | Max. Data Access Time from CL at CL = 2.5 (t _{AC}) | 0.7ns | 70h |
| 25 | Min. CLK Cycle Time at CL = 1.5 (t _{CYC}) | - | 00h |
| 26 | Max. Data Access Time from CL at CL = 1.5 (t _{AC}) | - | 00h |
| 27 | Minimum Row Precharge Time (t _{RP}) | 18ns | 48h |
| 28 | Minimum Row Active to Row Active (t _{RRD}) | 12ns | 30h |
| 29 | Minimum /RAS to /CAS Delay (t _{RCD}) | 18ns | 48h |
| 30 | Minimum /RAS Pulse Width (t _{RAS}) | 42ns | 2Ah |
| 31 | Module Rank Density | 512MB | 80h |
| 32 | Min. CMD/ADDR Signal Setup Time (t _{IS}) | 0.75ns | 80h |
| 33 | Min. CMD/ADDR Signal Hold Time (t _{IH}) | 0.75ns | 80h |
| 34 | Min. Data/Data Mask Input Setup Time (t _{DS}) | 0.45ns | 45h |
| 35 | Min. Data/Data Mast Input Hold Time (t _{DH}) | 0.45ns | 45h |

Serial Presence Detect Information continued on next page.

SERIAL PRESENCE DETECT INFORMATION *(continued)*Serial PD Interface Protocol; I²C; Current sink capability of SDA driver <= 3mA; Maximum Clock Frequency: 100KHz

| Byte | Description | Entry | Hex Value |
|---------|--|---|------------|
| 36-40 | Reserved for VCSDRAM | - | 00h |
| 41 | Row Cycle Time (^t RC) | 60ns | 3Ch |
| 42 | Auto Refresh Cycle Time (^t RFC) | 72ns | 48h |
| 43 | SDRAM Device Max. Cycle Time (^t CKMAX) | 12ns | 30h |
| 44 | DQS-DQ Skew Time (^t DQSQ) | 0.45ns | 2Dh |
| 45 | SDRAM Device Max. Read Data Hold Skew Factor (^t QHS) | 0.55ns | 55h |
| 46 | Reserved | - | 00h |
| 47 | DDR SDRAM DIMM Height | No DIMM Height Available | 00h |
| 48-61 | Reserved | - | 00h |
| 62 | SPD Revision | JEDEC Revision 1.0 | 10h |
| 63 | Checksum for Bytes 0 - 62 | JEDEC Calculation | xxh |
| 64 | Manufacturer's JEDEC ID Code per JEP-106E | Continuation Code | 7Fh |
| 65 | Manufacturer's JEDEC ID Code (continued) | STEC's ID | A8h |
| 66-71 | - | - | 00h |
| 72 | Manufacturing Location STEC USA (01h) STEC Malaysia | STEC USA (01h) STEC Malaysia (02h) | 01h 02h |
| 73-90 | Module Part Number (ASCII) | - | 00h |
| 91 | Module Revision Code | Engineering (00h) Rev. A (01h) Rev. B (02h) | xxh |
| 92 | - | - | 00h |
| 93 | Year of Manufacture (BCD) | Year (BCD) | yyh |
| 94 | Week of Manufacture (BCD) | Week (BCD) | wwh |
| 95 | Assembly Serial Number | Tester Number | ssh |
| 96 | | Serial # (Bits 7 - 0) | ssh |
| 97 | | Serial # (Bits 15 - 8) | ssh |
| 98 | | Serial # (Bits 23 - 16) | ssh |
| 99-127 | Manufacturer-Specific Data (RSVD) | - | xxh |
| 128-255 | Open for Customer Use | - | 00h |

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages and temperatures for extended periods may affect device reliability.

| Symbol | Parameter | Minimum | Maximum | Units |
|-------------------|---|---------|---------|-------|
| V_{IN}, V_{OUT} | Voltage on any Pin relative to V_{SS} | -1.0 | +3.6 | V |
| V_{DD} | V_{DD} Supply Voltage relative to V_{SS} | -1.0 | +3.6 | V |
| V_{DDQ} | V_{DDQ} Supply Voltage relative to V_{SS} | -1.0 | +3.6 | V |
| T_{STG} | Storage Temperature | -55 | +125 | °C |
| P_D | Power Dissipation | 12 | | W |
| I_{OS} | Short Circuit Current | 50 | | mA |

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

Recommended Operating Conditions. Voltage referenced to $V_{SS} = 0V$, $T_A = 0$ to $70^\circ C$.

| Symbol | Parameter | Minimum | Maximum | Units | Notes |
|--------------|---|------------------|------------------|-------|-------|
| T_A | Ambient Operating Temperature | | | | |
| | Commercial | N/A | N/A | - | |
| | Industrial | -40 | 85 | °C | |
| V_{DD} | Supply Voltage (For a device with a Nominal VDD of 2.5V) | 2.3 | 2.7 | V | |
| V_{DDQ} | I/O Supply Voltage | 2.3 | 2.7 | V | |
| V_{REF} | I/O Reference Voltage | $0.49 * V_{DDQ}$ | $0.51 * V_{DDQ}$ | V | 1 |
| V_{TT} | I/O Termination Voltage | $V_{REF} - 0.04$ | $V_{REF} + 0.04$ | V | 2 |
| $V_{IH}(DC)$ | Input Logic High Voltage | $V_{REF} + 0.15$ | $V_{DDQ} + 0.3$ | V | 4 |
| $V_{IL}(DC)$ | Input Logic Low Voltage | -0.3 | $V_{REF} - 0.15$ | V | 4 |
| $V_{IN}(DC)$ | Input Voltage Level, CK and /CK | -0.3 | $V_{DDQ} + 0.3$ | V | |
| $V_{ID}(DC)$ | Input Differential Voltage, CK and /CK | 0.36 | $V_{DDQ} + 0.6$ | V | 3 |
| I_L | Input Leakage Current: | | | | |
| | A, BA, /RAS, /CAS, /WE | -16 | 16 | μA | |
| | CKE, /S | -16 | 16 | | |
| | CK0, /CK0 | -4 | 4 | | |
| | CK1-2, /CK1-2 | -6 | 6 | | |
| | DM | -2 | 2 | | |
| I_{OZ} | Output Leakage Current: | | | | |
| | DQ, CB, DQS | -5 | 5 | μA | |
| I_{OH} | Output High Current: | | | | |
| | ($V_{OUT} = V_{DDQ} - 0.373V$, min V_{REF} , min V_{TT}) | -16.8 | - | mA | |
| I_{OL} | Output Low Current: | | | | |
| | ($V_{OUT} = V_{DDQ} - 0.373V$, max V_{REF} , max V_{TT}) | 16.8 | - | mA | |

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT) *(continued)*

Recommended Operating Conditions. Voltage referenced to VSS = 0V, T_A = 0 to 70°C.

Notes:

1. Includes $\pm 25\text{mV}$ margin for DC offset on V_{REF}, and a combined total of $\pm 50\text{mV}$ margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled to V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of $\leq 3\text{nH}$.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to the V_{REF} envelop that has been bandwidth limited to 200MHz.
5. The value of V_{IX} is expected to equal $0.5 * V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.
6. These characteristics obey the SSTL-2 Class II standards.

DC CHARACTERISTICS

Recommended Operating Conditions unless otherwise specified. The module IDD was calculated on the basis of the component IDD and can be measured differently according to the DQ loading capacity. $V_{DD} = 2.7V$, $T_A = 10^{\circ}C$.

| Symbol | Parameter/Condition | Maximum | Units | Notes |
|--------|---|---------|-------|-------|
| IDD0 | OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles. | 1,040 | mA | 1 |
| IDD1 | OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0mA$; Address and control inputs changing once per clock cycle. | 1,280 | mA | 1 |
| IDD2P | PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK(MIN)}$; CKE = (LOW). | 40 | mA | 2 |
| IDD2F | IDLE STANDBY CURRENT: $/CS = HIGH$; All banks idle; $t_{CK} = t_{CK(MIN)}$; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM. | 360 | mA | 2 |
| IDD3P | ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK(MIN)}$; CKE = LOW. | 280 | mA | 2 |
| IDD3N | ACTIVE STANDBY CURRENT: $/CS = HIGH$; CKE = HIGH; One bank; Active-Precharge; $t_{RC} = t_{RAS(MAX)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle. | 400 | mA | 2 |
| IDD4R | OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0mA$. | 1,320 | mA | 1 |
| IDD4W | OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle. | 1,400 | mA | 1 |
| IDD5 | AUTO REFRESH CURRENT: $t_{RC} = t_{RC(MIN)}$. | 2,320 | mA | 1 |
| IDD6 | SELF REFRESH CURRENT: CKE $\leq 0.2V$. | 40 | mA | 2 |
| IDD7 | OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; Address and control inputs change only during Active READ, or WRITE commands. | 3,240 | mA | 1 |

Notes:

1. In a module with more than one rank, IDD_n is calculated with one rank in IDD_n and the other ranks in IDD_{2P} .
2. All ranks in IDD_n
where n = corresponding IDD condition listed in the Symbol column
and Values shown for DDR SDRAM components only.

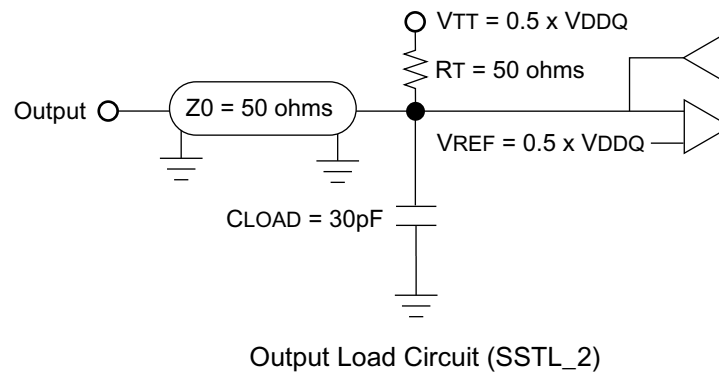
AC OPERATING CONDITIONS

 $V_{DD} = V_{DDQ} = 2.6V$; $T_A = 25^{\circ}C$, $f = 1MHz$

| Symbol | Parameter/Condition | Minimum | Maximum | Units | Notes |
|--------------|--|---------------------------|---------------------------|-------|-------|
| $V_{IH}(AC)$ | Input High (Logic 1) Voltage; DQ, DQS and DM Signals | $V_{REF} + 0.31$ | - | V | 3 |
| $V_{IL}(AC)$ | Input Low (Logic 0) Voltage; DQ, DQS and DM Signals | - | $V_{REF} - 0.31$ | V | 3 |
| $V_{ID}(AC)$ | Input Differential Voltage, CK and /CK Inputs | 0.7 | $V_{DDQ} + 0.6$ | V | 1 |
| $V_{IX}(AC)$ | Input Crossing Point Voltage, CK and /CK Inputs | $0.5 \cdot V_{DDQ} - 0.2$ | $0.5 \cdot V_{DDQ} + 0.2$ | V | 2 |

Notes:

- V_{ID} is the magnitude of the difference between the input level on CK and the input on /CK.
- The value of V_{IX} is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are a relation to a V_{REF} envelope that has been bandwidth limited 20MHz.



CAPACITANCE
 $V_{DD} = V_{DDQ} = 2.6V, T_A = 25^{\circ}C, f = 1MHz$

| Symbol | Parameter | Maximum | Units |
|-----------|---|---------|-------|
| C_{IN0} | Input Capacitance: A, BA, /RAS, /CAS, /WE (30 pF added for board) | 54 | pF |
| C_{IN1} | Input Capacitance: CKE, /S (30 pF added for board) | 54 | pF |
| C_{IN2} | Input Capacitance: CK0, /CK0 (15 pF added for board) | 21 | pF |
| C_{IN3} | Input Capacitance: CK1-2, /CK1-2 | 24 | pF |
| $C_{I/O}$ | I/O Capacitance: Data, DM and DQS (5 pF added for board) | 10 | pF |

AC TIMING PARAMETERS (These AC Characteristics were tested on the component.)

| Symbol | Parameter | Minimum | Maximum | Units |
|--------------------|---|---------|---------|-----------------|
| t _{CK} | Clock Cycle Time | | | |
| | CL = 3 | N/A | N/A | ns |
| | CL = 2.5 | 6 | 13 | ns |
| | CL = 2 | 7.5 | 13 | ns |
| t _{RC} | Row Cycle Time | 60 | - | ns |
| t _{RFC} | Refresh Row Cycle time | 72 | - | ns |
| t _{RAS} | Row Active Time | 42 | 70K | ns |
| t _{RCD} | /RAS to /CAS Delay | 15 | - | ns |
| t _{RP} | Row Precharge Time | 15 | - | ns |
| t _{RRD} | Row Active to Row Active Delay | 12 | - | ns |
| t _{WR} | Write Recovery Time | 15 | - | ns |
| t _{WTR} | Internal WRITE to READ Command Delay | 1 | - | t _{CK} |
| t _{CH} | Clock High Level Width | 0.45 | 0.55 | t _{CK} |
| t _{CL} | Clock Low Level Width | 0.45 | 0.55 | t _{CK} |
| t _{DQSK} | DQS-Out Access Time from CK, /CK | -0.6 | +0.6 | ns |
| t _{AC} | Output Data Access Time from CK, /CK | | | |
| | CL = 3 | N/A | N/A | ns |
| | CL = 2.5 | -0.70 | +0.70 | ns |
| | CL = 2 | -0.70 | +0.70 | ns |
| t _{DQSQ} | Data Strobe Edge to Output Data Edge | - | 0.45 | ns |
| t _{RPRE} | Read Preamble | 0.9 | 1.1 | t _{CK} |
| t _{RPST} | Read Postamble | 0.4 | 0.6 | t _{CK} |
| t _{DQSS} | CK to Valid DQS-IN | 0.75 | 1.25 | t _{CK} |
| t _{WPRES} | DQS-In Setup Time | 0 | - | ns |
| t _{WPRE} | Write Preamble | 0.25 | - | t _{CK} |
| t _{DSS} | DQS Falling Edge to CK Rising - Setup Time | 0.2 | - | t _{CK} |
| t _{DSH} | DQS Falling Edge from CK Rising - Hold Time | 0.2 | - | t _{CK} |
| t _{DQSH} | DQS-In High Level Width | 0.35 | - | t _{CK} |
| t _{DQSL} | DQS-In Low Level Width | 0.35 | - | t _{CK} |
| t _{IS} | Address and Control Input Setup Time | 0.75 | - | ns |
| t _{IH} | Address and Control Input Hold Time | 0.75 | - | ns |
| t _{HZ} | Data-Out High Impedance Time from CK, /CK | - | +0.7 | ns |
| t _{LZ} | Data-Out Low Impedance Time from CK, /CK | -0.7 | - | ns |
| t _{MRD} | Mode Register Set Cycle time | 12 | - | ns |
| t _{DS} | DQ and DM Setup Time to DQS | 0.45 | - | ns |
| t _{DH} | DQ and DM Hold Time to DQS | 0.45 | - | ns |
| t _{DIPW} | DQ and DM Input Pulse Width | 1.75 | - | ns |

AC Timing Parameters continued on next page.

AC TIMING PARAMETERS *(continued)*

| Symbol | Parameter | Minimum | Maximum | Units |
|------------|--|--|---------|----------|
| t_{IPW} | Control and Address Input Pulse Width (for each input) | 2.2 | - | ns |
| t_{XSNR} | Exit Self-Refresh to any Non-READ Command | | | |
| | 128Mb, 256Mb, 512Mb | 75 | - | ns |
| | 1Gb | N/A | - | ns |
| t_{XSRD} | Exit Self-Refresh to any READ Command | 200 | - | t_{CK} |
| t_{REFC} | REFRESH-to-REFRESH Command Interval | | | |
| | 128Mb | - | N/A | μs |
| | 256Mb, 512Mb, 1Gb | - | 70.3 | μs |
| t_{RFC} | AUTO REFRESH Command Period | | | |
| | 128Mb, 256Mb, 512Mb | 72 | - | μs |
| | 1Gb | N/A | - | μs |
| t_{REFI} | Average Periodic Refresh Interval | | | |
| | 128Mb | - | N/A | μs |
| | 256Mb, 512Mb, 1Gb | - | 7.8 | μs |
| t_{QH} | Output DQS Valid Window | $t_{HP} \text{ min} - t_{QHS}$ | | ns |
| t_{HP} | Clock Half Period | $t_{CL} \text{ min}$ or $t_{CH} \text{ min}$ | | ns |
| t_{QHS} | Data Hold Skew Factor | - | 0.55 | ns |
| t_{WPST} | DQS Write Postamble Time | 0.4 | 0.6 | t_{CK} |
| t_{RAP} | Active to Autoprecharge Delay | 15 | - | ns |
| t_{VTD} | Terminating Voltage Delay to VDD | - | - | ns |
| N/A | Data Valid Output Window | $t_{QH} - t_{DQSQ}$ | | ns |

Notes:

1. It is recommended that the system designers or system engineers reference the latest specification release notes from the DRAM manufactures pertaining to these signals. The default operational characteristics are listed here for reference only.

REVISION HISTORY

| Revision | Date | Description |
|-----------------|-------------|--------------------|
| -101 | 04/07/2009 | Initial release. |

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