

128M x 72 Bit (1GB) 184-Pin DDR Registered DIMM (PC2100) 2 Ranks x 8

FEATURES

- PC2100 Compliant (DDR266B or faster operated at 133MHz, 7.5ns, CL-^tRCD-^tRP: 2.5-3-3 Clks)
- 184-Pin RDIMM form factor
- Auto and Self-Refresh Capability (8,192 cycles/64ms refresh)
- +2.5V \pm 0.2 V_{DD} and V_{DDQ}
- DDR Architecture: Two data accesses per clock cycle, differential clock inputs (CK0, /CK0) and bidirectional differential data strobe (DQS)
- Four internal component banks for concurrent operation
- Auto Precharge option for each burst access
- Burst Lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect (SPD) EEPROM
- ECC
- Gold edge contacts

ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
ALC72E8M128M8M-B75EWSGU	2.5	266	2.1 GB/s

GENERAL DESCRIPTION

The ALC72E8M128M8M-B75EWSGU is a 128M x 72 bit (1GB) 184-pin Double Data Rate (DDR) Registered Dual In-Line Memory Module (RDIMM) with data ECC.

The module consists of eighteen CMOS 16M x 8 bit x 4 bank DDR SDRAMs in TSOP packages mounted in 2 ranks on a 184-pin glass epoxy substrate.

A serial EEPROM using the two pin I²C protocol is also mounted to provide the Serial Presence Detects (SPD). A PLL supplies clocks to the SDRAMs from one clock input. Decoupling capacitors are mounted across the power supply. Damping resistors are added in series for DQ, DQS and DM signals.

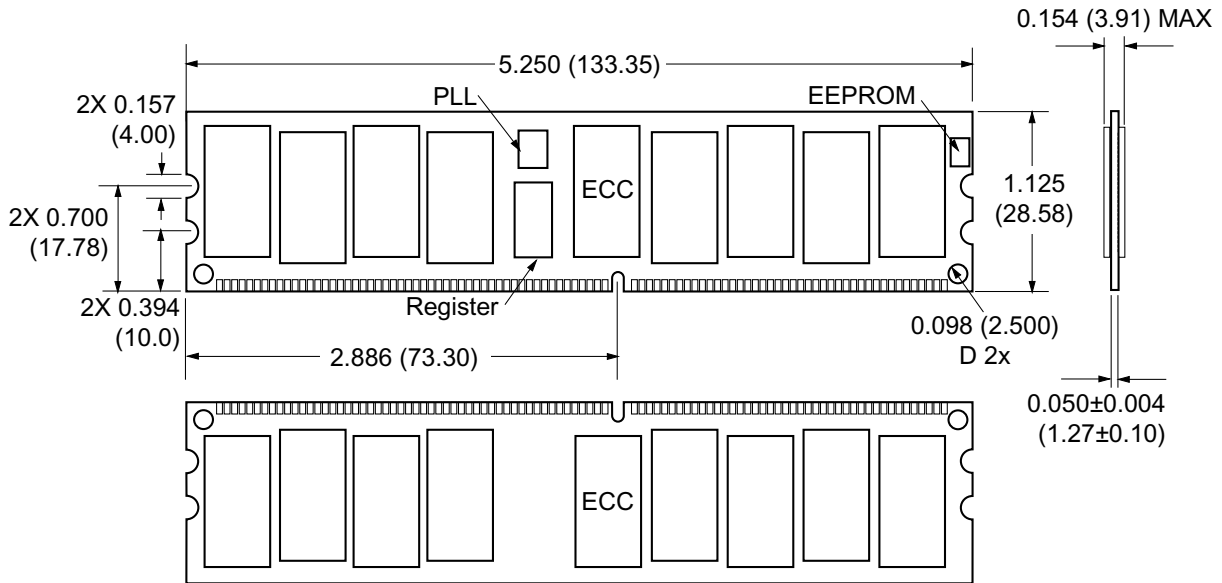
The module has gold edge connections and is intended for mounting into 184-pin RDIMM edge connector sockets keyed for 2.5V V_{DD} and V_{DDQ}.

DRAM MANUFACTURERS LIST

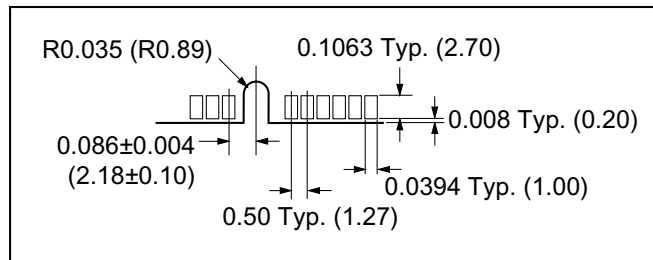
Manufacturer	Part Number	Die Rev
Samsung	K4H510838G-LCCC	G

PACKAGE DIMENSIONS *(Board No. 1047)*

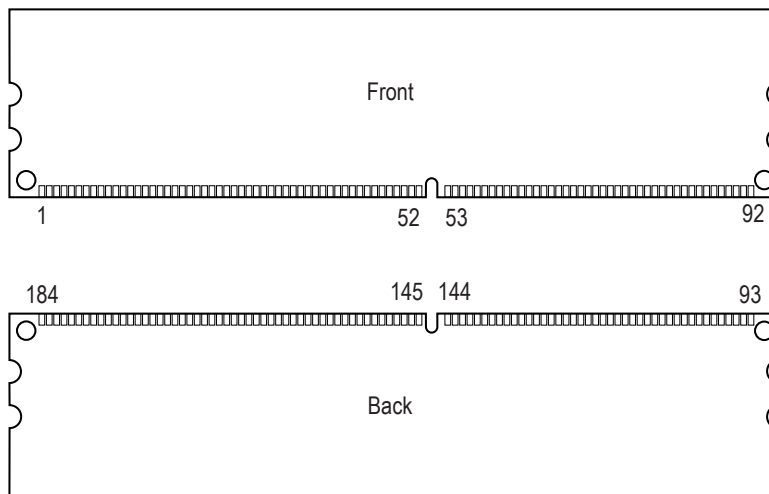
Units are in inches (millimeters). Tolerances are +0.005 (+0.127) unless otherwise specified.



Detail: Notch and Pad



PIN LOCATIONS



PIN CONFIGURATION (* = Not Used; / = Active Low; **Bold Line or Box** = Key)

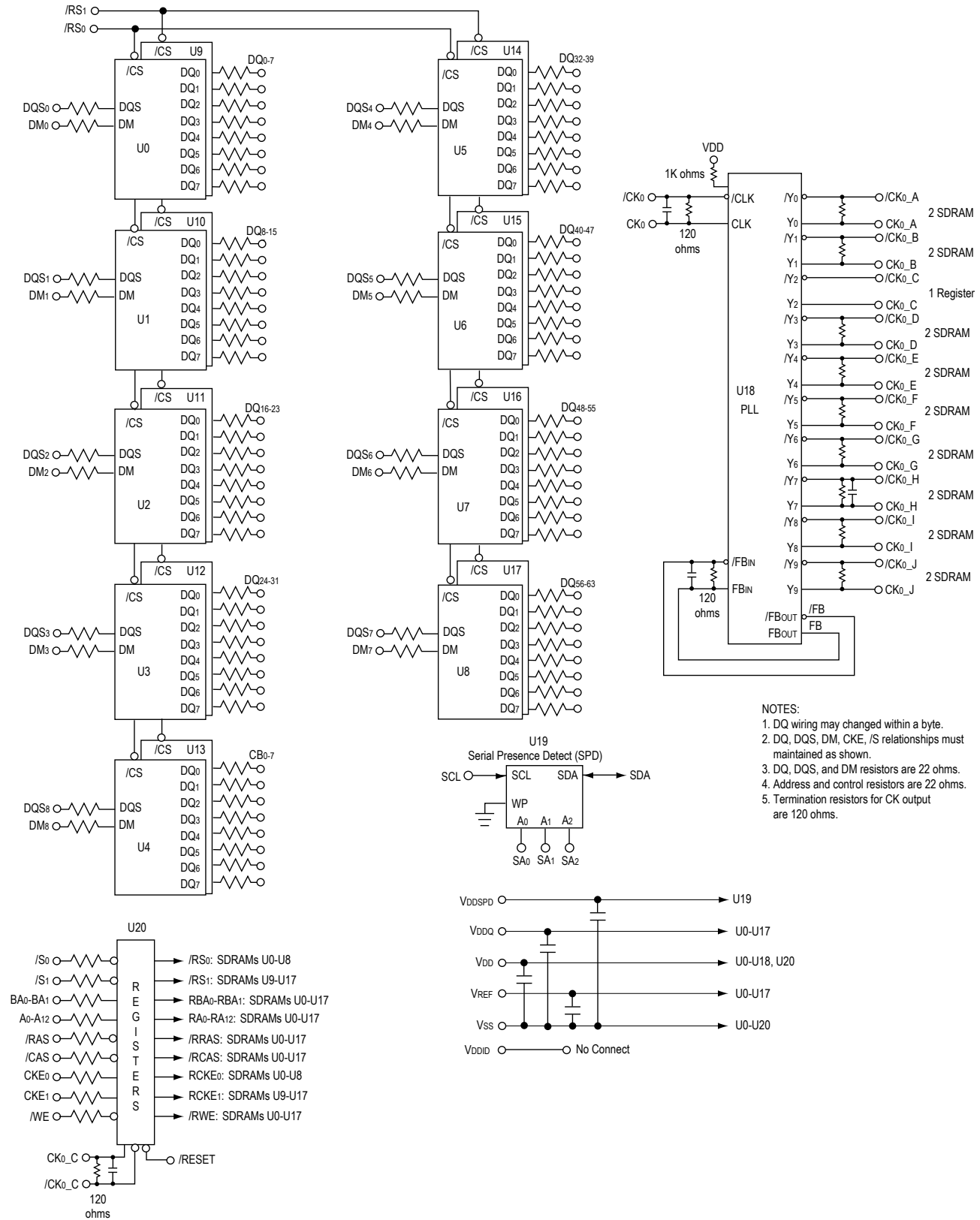
184-PIN DIMM PINOUT

184-Pin UDIMM Front Pinout								184-Pin UDIMM Back Pinout							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	24	DQ17	47	DQS8	70	VDD	93	VSS	116	VSS	139	VSS	162	DQ47
2	DQ0	25	DQS2	48	A0	71	/S2*	94	DQ4	117	DQ21	140	DM8	163	/S3*
3	VSS	26	VSS	49	CB2	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DM2	142	CB6	165	DQ52
5	DQS0	28	DQ18	51	CB3	74	VSS	97	DM0	120	VDD	143	VDDQ	166	DQS3
6	DQ2	29	A7	52	BA1	75	CK2	98	DQ6	121	DQ22	144	CB7	167	A13* (RFU)
7	VDD	30	VDDQ	53	DQ32	76	/CK2	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DM6
9	A15* (RFU)	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	NC	33	DQ24	56	DQS4	79	DQ50	102	NC (TEST*)	125	A6	148	VDD	171	DQ55
11	VSS	34	VSS	57	DQ34	80	DQ51	103	A13* (RFU)	126	DQ28	149	DM4	172	VDDQ
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	A14* (RFU)
13	DQ9	36	DQS3	59	BA0	82	VDDID	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DM3	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DM1	130	A3	153	DQ44	176	VSS
16	CK1*	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	/RAS	177	DM7
17	/CK1*	40	DQ27	63	/WE	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	/CAS	88	DQ59	111	CKE1	134	CB4	157	/S0	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	CB5	158	/S1	181	SA0
21	CKE0	44	CB0	67	DQS5	90	NC	113	BA2*	136	VDDQ	159	DM5	182	SA1
22	VDDQ	45	CB1	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115	A12	138	/CK0	161	DQ46	184	VDDSPD

PIN CONFIGURATION (Continued) (* = Not Used; / = Active Low)**PIN FUNCTIONS**

Symbol	Type	Function
CK0-CK1, /CK0*/-/CK1*	Input	Clock
CKE0, CEK1	Input	Clock Enable
/S0, /S1, /S2*, /S3*	Input	Chip Select
/RAS, /CAS, /WE	Input	Command Inputs (along with /S)
DM0-DM8	Input	Input Data Mask
BA0-BA1, BA2*	Input	Bank Address Inputs
A0-A12, A13*-A15*	Input	Address Inputs
DQ0-DQ63	Input/Output	Data
CB0-CB7	Input/Output	Check Bits
SCL	Input	Serial Clock for Presence Detect
SA0-SA2	Input	Presence Detect Address Inputs
SDA	Input/Output	Serial Presence Detect Data
NC		No Connect
RFU		Reserved for Future Use
VDDQ	Supply	DQ Power Supply: 2.5V ±0.2V
VDD	Supply	Power Supply: 2.5V ±0.2V
VSS	Supply	Ground
VREF	Supply	Reference Voltage
VDDSPD	Supply	Serial EEPROM Positive Power Supply 2.2V to +5.5V
VDDID	Output	VDD Identification Flag (NC for VDD=VDDQ)
TEST*		Memory Bus Test Tool (NC and not used for DIMMs)

FUNCTIONAL BLOCK DIAGRAM



- NOTES:
1. DQ wiring may be changed within a byte.
 2. DQ, DQS, DM, CKE, /S relationships must be maintained as shown.
 3. DQ, DQS, and DM resistors are 22 ohms.
 4. Address and control resistors are 22 ohms.
 5. Termination resistors for CK output are 120 ohms.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol; I²C; Current sink capability of SDA driver <= 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
0	Number of SPD Bytes used by Manufacturer	128	80h
1	Total Number of Bytes in SPD Device	256	08h
2	Fundamental Memory Type	DDR SDRAM	07h
3	Number of Row Addresses on Assembly	13	0Dh
4	Number of Column Addresses on Assembly	11	0Bh
5	Number of Physical Banks on Assembly	2	02h
6	Data Width of the Assembly	72	48h
7	...Data Width of the Assembly (continued)	-	00h
8	Module Voltage Interface Level	SSTL 2.5V	04h
9	SDRAM Cycle Time at CL = 2.5 (t _{CYC})	7.5ns	75h
10	SDRAM Access from Clock at CL = 2.5 (t _{AC})	0.75ns	75h
11	DIMM Configuration Type	Non-Addr/Cmd Parity ECC Data	02h
12	Refresh Rate/Type	7.8μs/Self-Refresh	82h
13	SDRAM Width	x8	08h
14	Error-Checking SDRAM Data Width	x8	08h
15	Min. CLK Delay for Back-to-Back Rand. Col. Addr.	t _{CCD} = 1 CLK	01h
16	Burst Lengths Supported	2, 4, 8	0Eh
17	Number of Banks on SDRAM Device	4	04h
18	CAS Latencies Supported	2, 2.5	0Ch
19	CS Latencies Supported	0	01h
20	Write Latencies Supported	1	02h
21	SDRAM Module Attributes	1 Register/1 PLL Differential Clock	26h
22	SDRAM Device Attributes: General	Fast/Concurrent AP	C0h
23	Min. CLK Cycle Time at CL = 2 (t _{CYC})	10ns	A0h
24	Max. Data Access Time from CL at CL = 2 (t _{AC})	0.75ns	75h
25	Min. CLK Cycle Time at CL = X (t _{CYC})	N/A	00h
26	Max. Data Access Time from CL at CL = X (t _{AC})	N/A	00h
27	Minimum Row Precharge Time (t _{RP})	20ns	50h
28	Minimum Row Active to Row Active (t _{RRD})	15ns	3Ch
29	Minimum /RAS to /CAS Delay (t _{RCD})	20ns	50h
30	Minimum /RAS Pulse Width (t _{RAS})	45ns	2Dh
31	Module Rank Density	512MB	80h
32	Min. CMD/ADDR Signal Setup Time (t _{IS})	0.90ns	90h
33	Min. CMD/ADDR Signal Hold Time (t _{IH})	0.90ns	90h
34	Min. Data/Data Mask Input Setup Time (t _{DS})	0.50ns	50h
35	Min. Data/Data Mast Input Hold Time (t _{DH})	0.50ns	50h

Serial Presence Detect Information continued on next page.

SERIAL PRESENCE DETECT INFORMATION (continued)Serial PD Interface Protocol; I²C; Current sink capability of SDA driver <= 3mA; Maximum Clock Frequency: 100KHz

Byte	Description	Entry	Hex Value
36-40	Reserved	-	00h
41	Row Cycle Time (t ^{RC})	65ns	41h
42	Auto Refresh Cycle Time (t ^{RFC})	75ns	4Bh
43	SDRAM Device Max. Cycle Time (t ^{CKMAX})	12ns	30h
44	DQS-DQ Skew Time (t ^{DQSQ})	0.5ns	32h
45	SDRAM Device Max. Read Data Hold Skew Factor (t ^{QHS})	0.75ns	75h
46	Reserved	-	00h
47	DDR SDRAM DIMM Height	1.125" to 1.25" (1.25")	01h
48-61	Reserved	-	00h
62	SPD Revision	JEDEC Revision 1.0	10h
63	Checksum for Bytes 0 - 62	JEDEC Calculation	xxh
64	Manufacturer's JEDEC ID Code per JEP-106E	Continuation Code	7Fh
65	Manufacturer's JEDEC ID Code (continued)	STEC's ID	A8h
66-71	-	-	00h
72	Manufacturing Location STEC USA (01h) STEC Malaysia	STEC USA (01h) STEC Malaysia (02h)	01h 02h
73-90	Module Part Number (ASCII)	-	00h
91	Module Revision Code	Engineering (00h) Rev. A (01h) Rev. B (02h)	01h
92	-	-	00h
93	Year of Manufacture (BCD)	Year (BCD)	yyh
94	Week of Manufacture (BCD)	Week (BCD)	wwh
95	Assembly Serial Number	Tester Number	ssh
96		Serial # (Bits 7 - 0)	ssh
97		Serial # (Bits 15 - 8)	ssh
98		Serial # (Bits 23 - 16)	ssh
99-127	Manufacturer-Specific Data (RSVD)	-	xxh
128-255	Open for Customer Use	-	00h

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages and temperatures for extended periods may affect device reliability.

Symbol	Parameter	Minimum	Maximum	Units
V_{IN}, V_{OUT}	Voltage on any Pin relative to V_{SS}	-0.5	+3.6	V
V_{DD}	V_{DD} Supply Voltage relative to V_{SS}	-1.0	+3.6	V
V_{DDQ}	V_{DDQ} Supply Voltage relative to V_{SS}	-1.0	+3.6	V
T_{STG}	Storage Temperature	-55	+150	°C
P_D	Power Dissipation	27		W
I_{OS}	Short Circuit Current	50		mA

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT)Recommended Operating Conditions. Voltage referenced to VSS = 0V, T_A = 0 to 70°C.

Symbol	Parameter	Minimum	Maximum	Units	Notes
V _{DD}	Supply Voltage (For a device with a Nominal VDD of 2.5V)	2.3	2.7	V	
V _{DDQ}	I/O Supply Voltage	2.3	2.7	V	
V _{REF}	I/O Reference Voltage	V _{DDQ} /2 -50mV	V _{DDQ} /2 +50mV	V	1
V _{TT}	I/O Termination Voltage	V _{REF} -0.04	V _{REF} +0.04	V	2
V _{IH} (DC)	Input Logic High Voltage	V _{REF} +0.15	V _{DDQ} +0.3	V	4
V _{IL} (DC)	Input Logic Low Voltage	-0.3	V _{REF} -0.15	V	4
V _{IN} (DC)	Input Voltage Level, CK and /CK	-0.3	V _{DDQ} +0.3	V	
V _{ID} (DC)	Input Differential Voltage, CK and /CK	0.36	V _{DDQ} +0.6	V	3
I _L	Input Leakage Current			μA	
	A, BA, /RAS, /CAS, /WE (Register Input)	-5	5	μA	
	CKE, /S (Register Input)	-5	5	μA	
	CK0, /CK0 (PLL Input)	-5	5	μA	
	DM	-10	10	μA	
I _{OZ}	Output Leakage Current	-10	10	μA	
I _{OH}	Output High Current (V _{OUT} = V _{TT} + 0.84V) (Normal Strength Driver)	-16.8	-	mA	
I _{OL}	Output Low Current (V _{OUT} = V _{TT} - 0.84V) (Normal Strength Driver)	16.8	-	mA	
IOH	Output High Current (V _{OUT} = V _{TT} + 0.45V) (Half Strength Driver)	-9	-	mA	
IOL	Output Low Current (V _{OUT} = V _{TT} - 0.45V) (Half Strength Driver)	9	-	mA	

Notes:

- Includes ±25mV margin for DC offset on V_{REF}, and a combined total of ±50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled to V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤3nH.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to the V_{REF} envelop that has been bandwidth limited to 200MHz.

DC CHARACTERISTICS

Recommended Operating Conditions unless otherwise specified. The module IDD was calculated on the basis of the component IDD and can be measured differently according to the DQ loading capacity. $V_{DD} = 2.7V$, $T_A = 10^{\circ}C$.

Symbol	Parameter/Condition	Maximum	Units
IDD0	OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	630	mA
IDD1	OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0mA$; Address and control inputs changing once per clock cycle.	765	mA
IDD2P	PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK(MIN)}$; CKE = (LOW).	90	mA
IDD2F	IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; $t_{CK} = t_{CKMIN}$; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM.	414	mA
IDD3P	ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK(MIN)}$; CKE = LOW.	360	mA
IDD3N	ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; $t_{RC} = t_{RAS(MAX)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	720	mA
IDD4R	OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0mA$.	900	mA
IDD4W	OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle.	945	mA
IDD5	AUTO REFRESH CURRENT: $t_{RC} = t_{RC(MIN)}$.	1,035	mA
IDD6	SELF REFRESH CURRENT: CKE $\leq 0.2V$.	90	mA
IDD7	OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; Address and control inputs change only during Active READ, or WRITE commands.	2,025	mA

Notes:

1. Values shown for DDR SDRAM components only.
2. Values will differ depending on DRAM parts used on the module.
3. IDD values are calculated using worst case specifications of currently available DRAMs from different manufacturers.
4. For a one rank module:
 IDDn is calculated with the rank in IDDn.
 For two rank module:
 IDD0, IDD1, IDD4W, IDD4R, IDD5 and IDD7 are calculated with one rank in IDDn and one rank in IDD2P **and** IDD2P, IDD2Q, IDD2N, IDD3P, IDD3N and IDD6 are calculated with two ranks in IDDn.

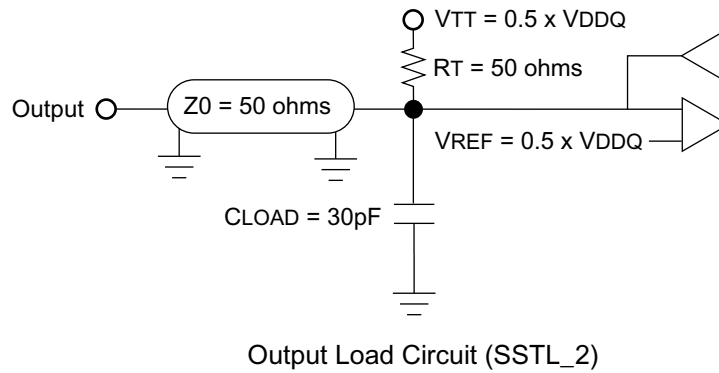
AC OPERATING CONDITIONS

$V_{DD} = V_{DDQ} = 2.6V$; $T_A = 25^{\circ}C$, $f = 1MHz$

Symbol	Parameter/Condition	Minimum	Maximum	Units	Notes
$V_{IH}(AC)$	Input High (Logic 1) Voltage; DQ, DQS and DM Signals	$V_{REF} + 0.31$	-	V	3
$V_{IL}(AC)$	Input Low (Logic 0) Voltage; DQ, DQS and DM Signals	-	$V_{REF} - 0.31$	V	3
$V_{ID}(AC)$	Input Differential Voltage, CK and /CK Inputs	0.7	$V_{DDQ} + 0.6$	V	1
$V_{IX}(AC)$	Input Crossing Point Voltage, CK and /CK Inputs	$0.5 \cdot V_{DDQ} - 0.2$	$0.5 \cdot V_{DDQ} + 0.2$	V	2

Notes:

1. V_{ID} is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of V_{IX} is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are a relation to a V_{REF} envelope that has been bandwidth limited 20MHz.



CAPACITANCE
 $V_{DD} = V_{DDQ} = 2.5V, T_A = 25^{\circ}C, f = 1MHz$

Symbol	Parameter	Maximum	Units
C_{CK0}	Input Capacitance: CK0, /CK0 (15pF added for board)	8.5	pF
C_{I0}	Input Capacitance: BA, A, /RAS, /CAS, /WE, /S, CKE, ODT (5pF added for board, Registered Input)	8	pF
$C_{I/O}$	Input/Output Capacitance: DQ, CB, DQS, /DQS, DM (5pF added for board)	15	pF

AC TIMING PARAMETERS (These AC Characteristics were tested on the component.)

Symbol	Parameter	Minimum	Maximum	Units
t_{CK}	Clock Cycle Time			
	CL = 3	N/A	N/A	ns
	CL = 2.5	7.5	12	ns
	CL = 2	10	12	ns
t_{RC}	Row Cycle Time	65	-	ns
t_{RFC}	Refresh Row Cycle time	75	-	ns
t_{RAS}	Row Active Time	45	70K	ns
t_{RCD}	/RAS to /CAS Delay	20	-	ns
t_{RP}	Row Precharge Time	20	-	ns
t_{RRD}	Row Active to Row Active Delay	15	-	ns
t_{WR}	Write Recovery Time	15	-	ns
t_{WTR}	Internal WRITE to READ Command Delay	1	-	t_{CK}
t_{CH}	Clock High Level Width	0.45	0.55	t_{CK}
t_{CL}	Clock Low Level Width	0.45	0.55	t_{CK}
t_{DQSCK}	DQS-Out Access Time from CK, /CK	-0.75	+0.75	ns
t_{AC}	Output Data Access Time from CK, /CK			
	CL = 3	N/A	N/A	ns
	CL = 2.5	-0.75	+0.75	ns
	CL = 2	-0.75	+0.75	ns
t_{DQSQ}	Data Strobe Edge to Output Data Edge	-	0.5	ns
t_{RPRE}	Read Preamble	0.9	1.1	t_{CK}
t_{RPST}	Read Postamble	0.4	0.6	t_{CK}
t_{DQSS}	CK to Valid DQS-IN	0.75	1.25	t_{CK}
t_{WPRES}	DQS-In Setup Time	0	-	ns
t_{WPRE}	Write Preamble	0.25	-	t_{CK}
t_{DSS}	DQS Falling Edge to CK Rising - Setup Time	0.2	-	t_{CK}
t_{DSH}	DQS Falling Edge from CK Rising - Hold Time	0.2	-	t_{CK}
t_{DQSH}	DQS-In High Level Width	0.35	-	t_{CK}
t_{DQSL}	DQS-In Low Level Width	0.35	-	t_{CK}
t_{IS}	Address and Control Input Setup Time	0.9	-	ns
t_{IH}	Address and Control Input Hold Time	0.9	-	ns
t_{HZ}	Data-Out High Impedance Time from CK, /CK	$t_{AC} \text{ max}$		ns
t_{LZ}	Data-Out Low Impedance Time from CK, /CK	$t_{AC} \text{ min}$		ns
t_{MRD}	Mode Register Set Cycle time	15	-	ns
t_{DS}	DQ and DM Setup Time to DQS	0.5	-	ns
t_{DH}	DQ and DM Hold Time to DQS	0.5	-	ns
t_{DIPW}	DQ and DM Input Pulse Width	1.75	-	ns

AC Timing Parameters continued on next page.

AC TIMING PARAMETERS *(continued)*

Symbol	Parameter	Minimum	Maximum	Units
t _{IPW}	Control and Address Input Pulse Width (for each input)	2.2	-	ns
t _{XSNR}	Exit Self-Refresh to any Non-READ Command			
	128Mb, 256Mb, 512Mb	75	-	ns
	1Gb	N/A	-	ns
t _{XSRD}	Exit Self-Refresh to any READ Command	200	-	t _{CK}
t _{REFC}	REFRESH-to-REFRESH Command Interval			
	128Mb	-	N/A	μs
	256Mb, 512Mb, 1Gb	-	70.3	μs
t _{RFC}	AUTO REFRESH Command Period			
	128Mb, 256Mb, 512Mb	75	-	μs
	1Gb	N/A	-	μs
t _{REFI}	Average Periodic Refresh Interval			
	128Mb	-	N/A	μs
	256Mb, 512Mb, 1Gb	-	7.8	μs
t _{QH}	Output DQS Valid Window	t _{HP min} - t _{QHS}		ns
t _{HP}	Clock Half Period	t _{CL min} or t _{CH min}		ns
t _{QHS}	Data Hold Skew Factor	-	0.75	ns
t _{WPST}	DQS Write Postamble Time	0.4	0.6	t _{CK}
t _{RAP}	Active to Autoprecharge Delay	20	-	ns
t _{VTD}	Terminating Voltage Delay to VDD	0	-	ns
N/A	Data Valid Output Window	t _{QH} - t _{DQSQ}		ns

Notes:

1. It is recommended that the system designers or system engineers reference the latest specification release notes from the DRAM manufactures pertaining to these signals. The default operational characteristics are listed here for reference only.

REVISION HISTORY

Revision	Date	Description
-101	11/02/2009	Initial release.

DISCLAIMER OF LIABILITY

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